Three level inverter-based unified power flow controller

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Abstract: Unified power flow controller is a power electronics-based device utilised to improve transmission line capacity and control power flow transmitted by power transmission systems. This paper presents the application of the decoupled control strategy to control independently active and reactive power in the event of changes in the step points of the powers. Two types of controllers are used to handle the control strategy proposed: conventional PI regulator and fuzzy logic PI regulator. The fuzzy logic controller must have high performance to handle the problem of adjustment of power decoupling. Also, a three level neutral point controller inverter is used in both series and shunt parts of the UPFC to get multistep voltage wave and improve the power quality.

Keywords: GTO; power flow control; unified power flow controller; UPFC; FACTS.

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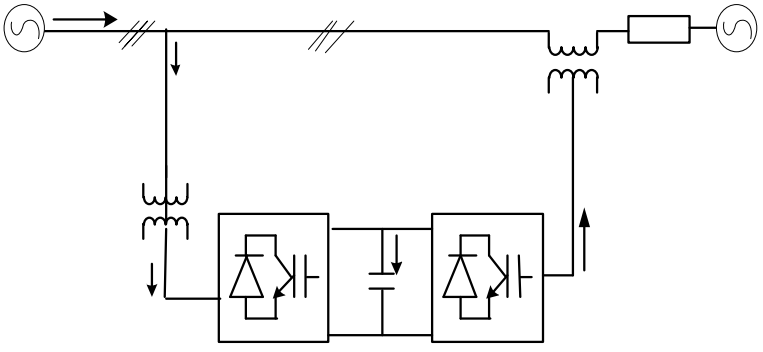
1 Introduction

The unified power flow controller (UPFC) is a power electronics-based device (Yam and Haque, 2004; Saribulut et al., 2011); it consists of two voltage source converters (SVC) connected together in back to back. The UPFC is coupled to the transmission line by means of two power transformers: the first one connects one of the VSC in series with the transmission line and the second connects the other VSC in shunt (Figure 1) (Yam and Haque, 2004; Naveena Bhargavi, 2013; Zhang et al., 2005; Vural and Tumay, 2007). The role of the UPFC is to control the power flow through the line in which is connected by influencing its parameters (voltage magnitude of each line ends, the phase angle between the voltage ends of the line and the reactance of line) (Naveena Bhargavi, 2013; Zhang et al., 2005; Berrahal et al., 2016; Vural and Tumay, 2007).

Figure 1 Unified power flow controller



The VSC is the key element of the UPFC; the conventional ones generate a rectangle wave voltage of two levels. For high voltage levels, a near sinusoidal wave is required for flexible operation of the power system. The use of multilevel converters seems to be the way to have additional levels in the voltage wave. The diode clamped multilevel inverter is a topology used for high voltage applications and have been proposed for the UPFC because it allows access for the DC link of the VSCs connected in back to back (Papic, 2000; Vural and Tumay, 2007). IGBT technology is used for the multilevel structure

(Taher et al., 2009; Liu et al., 2005). PWM multi carrier control strategy is the extension of the PWM algorithm to control the individual switches in multilevel topologies and is capable of generating multilevel voltage waveforms with reduced power loss within the converter (Ucar and Ozdemir, 2008; Bouhali et al., 2007).

The objective of this paper is to present an investigation of a UPFC based on three-level diode-clamped inverter to control power flow on one line transmission system. Phase-shifted sinusoidal PWM control algorithm is employed to control the two inverters switches. A synchronous d-q reference frame-based model of a UPFC is derived and the decoupled control circuits of the system are presented, two types of PI regulators are used to realise the decoupled control strategy. Finally, simulation results are presented to show the flexibility and performance of the proposed system.

2 Operating principle of the UPFC

The series converter of the UPFC injects a compensating voltage V_{se} that is at any angle with the prevailing line current (I) (Papic, 2000). The series injected voltage V_{se} has active (V_d) and reactive (V_q) components with load convention (Saribulut et al., 2011; Papic, 2000). The compensating voltage V_{se} exchange active and reactive powers, which are defined as:

$$P_{exch} = -V_{se} \cdot I = -V_{dq} \cdot I = V_d I \tag{1}$$

$$Q_{exch} = \left|-V_{se} * I\right| = \left|V_{dq} * I\right| = V_q \tag{2}$$

The voltage produced by the shunt converter is controllable in phase and amplitude. When this voltage is less than the line voltage, the shunt converter absorbs reactive power, the current flows from the line to the storage circuit via the inverter. If the shunt`s converter output voltage is greater than the line voltage, then it generates reactive power to the line in the form of current flowing from the inverter to the line (Papic, 2000; Berrahal et al., 2016).

3 Power line with UPFC modelling

Figure 2 shows the equivalent circuit model of a transmission line equipped with an UPFC. The nonlinearity caused by the semi-conductors devices, the transformer saturation and controller time delays are neglected in the equivalent circuit. Also, it is assumed that the transmission system is symmetrical.

The series and shunt VSIs are represented by controllable voltage source V_{se} and V_{sh}, respectively. R_{se} and L_{se} represent the resistance and leakage reactance of the series transformer and R_{sh} and L_{sh} represent the resistance and leakage reactance of shunt transformer.

The shunt injected current is:

$$\tilde{I}_{sh} = \frac{\tilde{V}_{sh} - \tilde{V}_{s1}}{jX_{sh}} \tag{3}$$

where X_{sh} is the transformer reactance.

The power injected by the shunt converter is:

$$P_{sh} = \frac{3}{2}\left(V_{sh\,d} I_{sh\,d} + V_{sh\,q} I_{sh\,q}\right) \tag{4}$$

The current injected by the series inverter is given by:

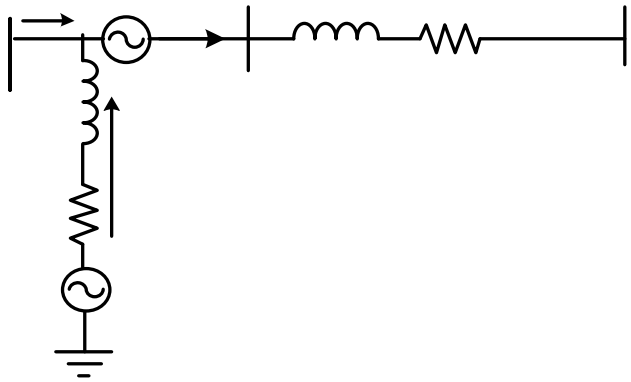
$$\tilde{I}_{se} = \frac{\tilde{V}_{s1} - \left(\tilde{V}_{se} + \tilde{V}_{R}\right)}{jX_{se}} \tag{5}$$

The power injected by the series converter is:

$$P_{se} = \frac{3}{2}\left(V_{se\,d} I_{se\,d} + V_{se\,q} I_{se\,q}\right) \tag{6}$$

The dynamic model of UPFC is derived by performing standard d-q transformation of the current through the series transformer and shunt transformer (Gholipour and Saadate, 2005; Fujita et al., 2006). They are given below (ω is the angular frequency of the voltages and currents (Ucar and Ozdemir, 2008).

Figure 2 Single phase representation of three phases UPFC system



3.1 Series part of the system model

The current of the series part is represented by equation (7):

$$\begin{aligned} \frac{d}{dt} i_{se\,d} &= -\frac{R_{se}}{L_{se}} i_{se\,q} - \frac{\omega}{L_{se}} V_{se\,d} \\ \frac{d}{dt} i_{se\,q} &= -\frac{R_{se}}{L_{se}} i_{se\,d} - \frac{\omega}{L_{se}} V_{se\,q} \end{aligned} \tag{7}$$

3.2 Shunt part of the system model

The current of the series part is represented by equation (8):

$$\begin{aligned}\frac{d}{dt}i_{sh\,d} &= -\frac{R_{sh}}{L_{sh}}i_{se\,q} - \frac{\omega}{L_{sh}}V_{sh\,d}\\ \frac{d}{dt}i_{se\,q} &= -\frac{R_{sh}}{L_{sh}}i_{sh\,d} - \frac{\omega}{L_{sh}}V_{sh\,q}\end{aligned} \tag{8}$$

3.3 DC circuit model

The DC circuit model will be formed from the principal of the equivalence of the active power between the DC bus and the AC bus of the UPFC (Papic, 2000; Berrahal et al., 2016).

The active power of the DC circuit is expressed by:

$$P_{dc} = V_{dc} I_{dc} \tag{9}$$

Also, the current through the capacitor is given by:

$$I_{dc} = C\frac{d}{dt}V_{dc} \tag{10}$$

where I_{dc} is the current flowing into the capacitor from the VSIs and C is the capacitance of the DC capacitor.

So, the active power of the DC circuit is:

$$P_{dc} = V_{dc} C\frac{d}{dt}V_{dc} \tag{11}$$

The AC power on the AC side of the DC circuit is equal to the total AC instantaneous active power delivered by the shunt and series converter.

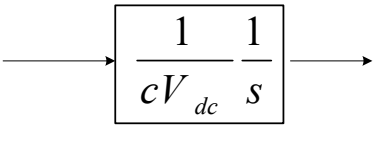
$$P_{AC} = \frac{3}{2}\left(V_{sh\,d}I_{sh\,d} + V_{sh\,q}I_{sh\,q} + V_{se\,d}I_{se\,d} + V_{se\,q}I_{se\,q}\right) \tag{12}$$

From equations (11) and (12), we get the DC voltage equation

$$\frac{d}{dt}V_{dc} = \frac{1}{CV_{dc}}\frac{3}{2}\left(V_{sh\,d}I_{sh\,d} + V_{sh\,q}I_{sh\,q} + V_{se\,d}I_{se\,d} + V_{se\,q}I_{se\,q}\right) \tag{13}$$

The block diagram of the DC link voltage is shown in Figure 3.

Figure 3 DC link dynamics



4 Conventional control strategy for UPFC

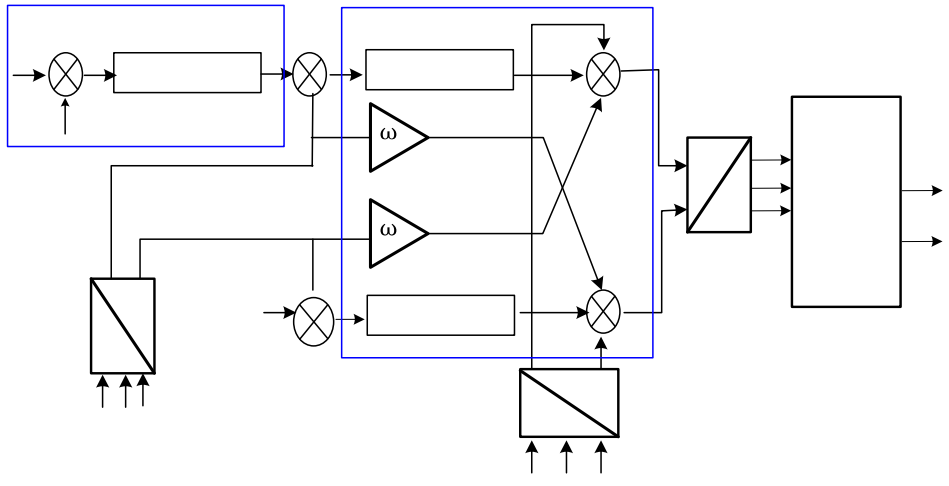
4.1 Shunt inverter control

The shunt inverter (STATCOM) injects a controlled shunt current by varying the shunt inverter voltage. It is responsible for AC-bus and DC-link voltage control (Liu et al., 2005; Dai et al., 2001; Farivar et al., 2016). The three phases current $I_{sh(a,b,c)}$ and voltage $V_{sh(a,b,c)}$ are converted to d and q parameters using Park's transformation. The $I_{sh\ ref}$ currents are calculated from the load voltage and the active and reactive power references desired by the load as given in equation (14).

$$i_{sd}^{ref} = \frac{2}{3}\frac{\left(p_s^{ref}V_d - q_s^{ref}V_q\right)}{V_d^2 + V_q^2}$$
$$i_{sq}^{ref} = \frac{2}{3}\frac{\left(p_s^{ref}V_q - q_s^{ref}V_d\right)}{V_d^2 + V_q^2} \tag{14}$$

The reference currents are compared to the shunt converter current and the error signals are the inputs for two PI controllers; the outputs represent the references of the PWM inverter control as shown on Figure 4.

Figure 4 Shunt inverter control structure for UPFC (see online version for colours)



The *dc* voltage bus is compared to *dc* voltage reference; the error signal fed a PI controller that gives the active power reference $P_{sh\ ref}$.

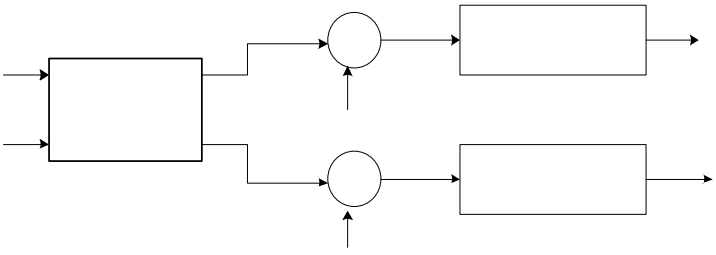
4.2 Series inverter control

As similar to the shunt converter, the current references are computed from the desired power references and the load voltage as given in equation.

The power flow control is then realised by using appropriately designed controllers to force the line currents to track their respective reference values. Two PI controllers are

used for this purpose. These controllers' outputs are the voltage references compared to the PWM carriers. The control system diagram is shown in Figure 5.

Figure 5 Series' inverter control structure for UPFC

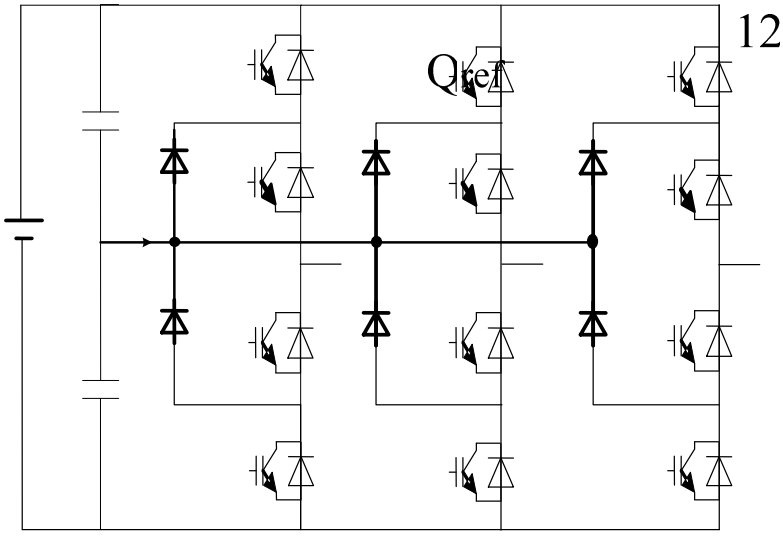


5 Inverter analysis

Multi level inverters have been widely used for power compensators to make them suitable for medium and high power applications.

Diode clamped multilevel inverter is a very general and widely used topology. This topology works on the concept of using diodes to limit voltage stress on power switches to synthesise a sinusoidal voltage from several voltage levels obtained from *dc* sources (Xie et al., 2012; Bouhali et al., 2007). Figure 6 shown the circuit of three level three phases neutral point (NPC) inverter used for the UPFC in this work.

Figure 6 Circuit of three phases three levels diode clamped inverter



The circuit comprises four switches disposed as S_{a1}, S_{a2}, S_{a3} and S_{a4} for phase *a*, as well for the phases *b* and *c*. Each leg comprises also two clamping diodes to limit voltage

stress on the switches (Taher et al., 2009; Bouhali et al., 2007) (Figure 6). The DC side is made up from two capacitors sharing the same NPC. The voltage across each capacitor is $V_{dc}/2$ and hence each switch limits a stress voltage of $V_{dc}/2$ value.

The switches turn on and off for every period, according to the mode shown in Table 1. Switches S_{a1}, S_{a3} and S_{a2}, S_{a4} are mixed in pairs.

Table 1 Switching states and output voltages of three-level diode clamped inverter

Sx1	*Sx2*	*Sx3*	*Sx4*	*Output voltage*
On	On	Off	Off	$V_{dc}/2$
Off	On	On	Off	0
Off	Off	On	On	$-V_{dc}/2$

6 Mathematical model of the inverter

The inverter output voltage is given by (Bouhali et al., 2007)

$$\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} F_{11}F_{12} & -F_{13}F_{14} \\ F_{21}F_{22} & -F_{23}F_{24} \\ F_{31}F_{32} & -F_{33}F_{34} \end{bmatrix}\begin{bmatrix} V_{c2} \\ V_{c2} \end{bmatrix} \tag{15}$$

where

F_{kj} is the switching function defining the state of the switch (1 if closed and 0 if open).

K number of the arm $k = 1, 2, 3$

j number of the switches in the arm $j = 1, 2, 3, 4$.

The current in the *dc* circuit are expressed as:

$$\begin{aligned} i_{c1} &= F_{11}F_{12}i_a + F_{21}F_{22}i_b + F_{31}F_{32}i_c \\ i_{c2} &= F_{13}F_{14}i_a + F_{23}F_{24}i_b + F_{33}F_{34}i_c \end{aligned} \tag{16}$$

7 The inverter control

The technique used for the inverter is the phase-shifted multi-carrier algorithm. As shown in Figure 7, two reference sine waves are compared with two triangle carriers disposed in anti-phases, when the instantaneous value of the triangular wave is less than the sine wave; the PWM output signal is in high level (1). Otherwise, it is turned into the low level (0).

The first and second signals of Figure 7 represent the PWM signals for the switches S_{a1} and S_{a3}, respectively; we see that these two signals are complimentary. The third one is the PWM signal of the switch S_{a2} and the last one correspond to the S_{a4} switch.

Figure 8 shows the line to line voltage of the three-level inverter, the output voltage signal is built up of many levels.

Figure 7 Two carriers pulse width modulation technique (see online version for colours)

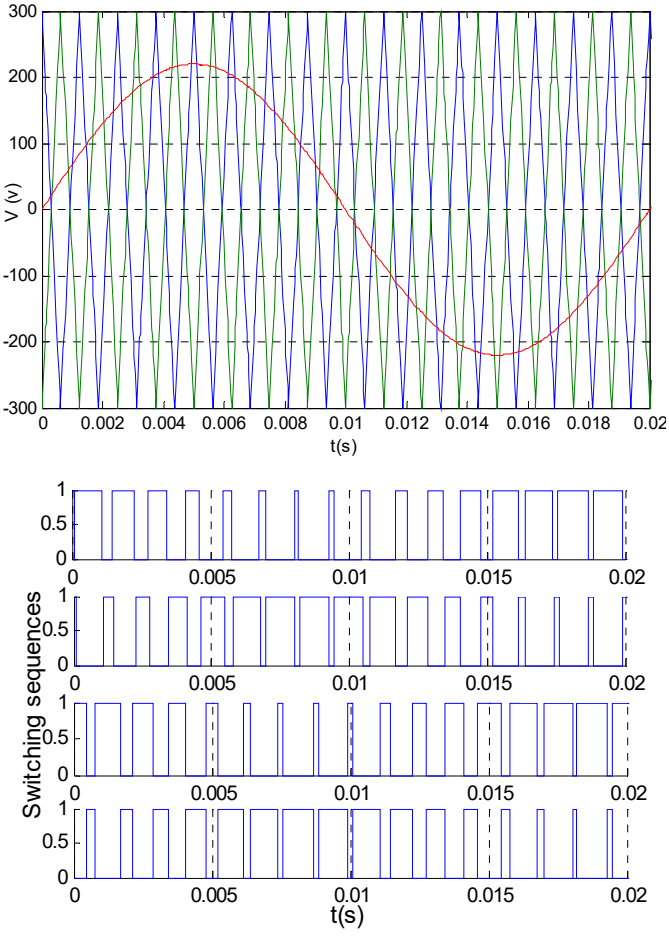
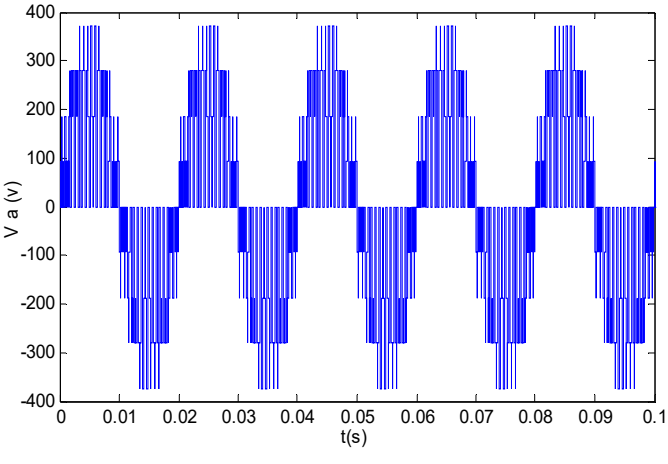


Figure 8 Line to line voltage of the inverter (see online version for colours)



8 Case study

The derived basic control of the UPFC was tested with MATLAB code program. A simplified network with two ports connected by one transmission line was used (Figure 2).

The performance of the proposed control is evaluated through digital simulations.

The system parameters used in simulation are:

$$R_{se} = 0.8\Omega,\ L_{se} = 10\ \text{mH},\ R_{sh} = 0.4\Omega,\ L_{sh} = 10\ \text{mH}$$

$$V_s = 220\ \text{V},\ V_r = 220\ \text{V},\ V_{dc} = 400\ \text{V},\ f = 50_{\text{Hz}},\ C = 2000_{\mu\text{F}}.$$

By analysing the simulation results for a step change in series reactive power reference from zero to 0.5 (pu) at t = 0.25 sec; a second change in the shunt active power reference from zero to 0.5 (pu) at t = 0.25sec; finally, a step change in series active power reference from –0.5 (pu) to +0.5 (pu) at t = 0.7 sec.

Figure 9 Series part of UPFC active and reactive power traces (see online version for colours)

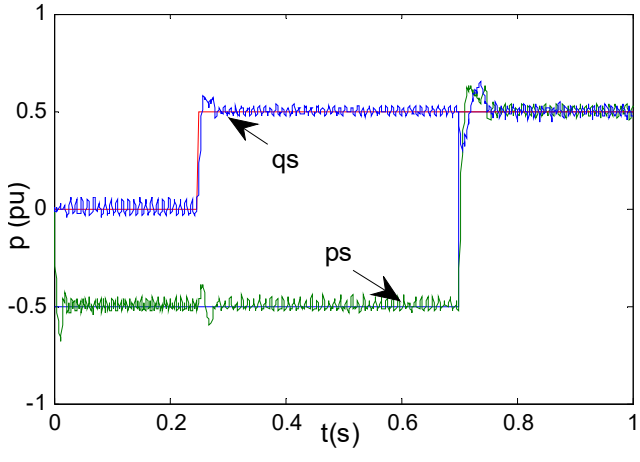


Figure 10 Active power of the shunt part of the UPFC (see online version for colours)

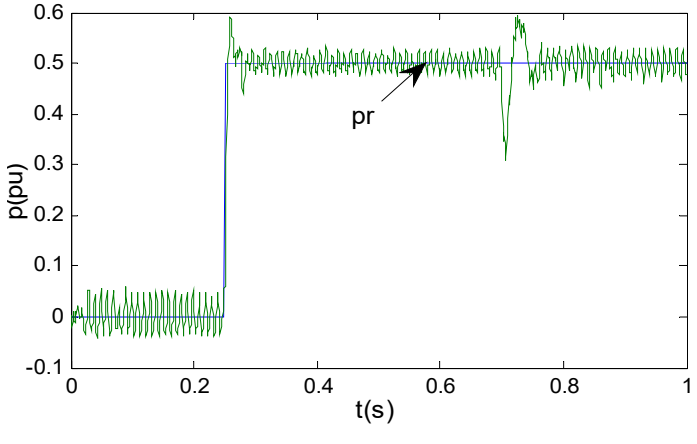


Figure 11 Power of the series' inverter (see online version for colours)

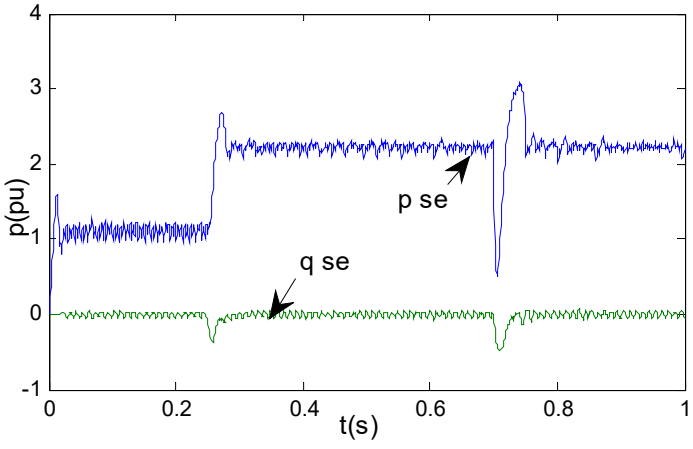
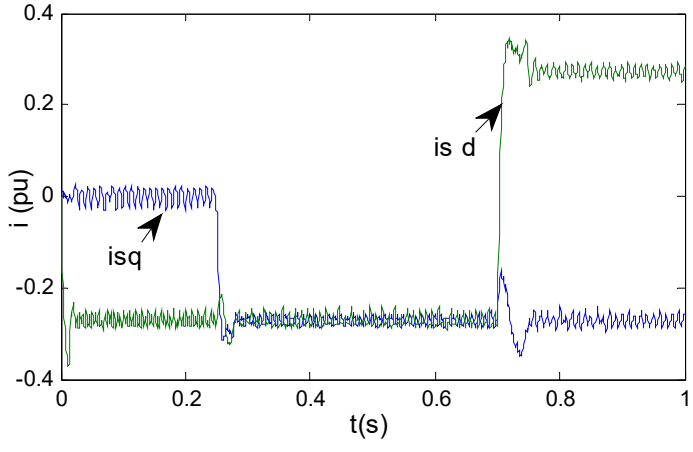
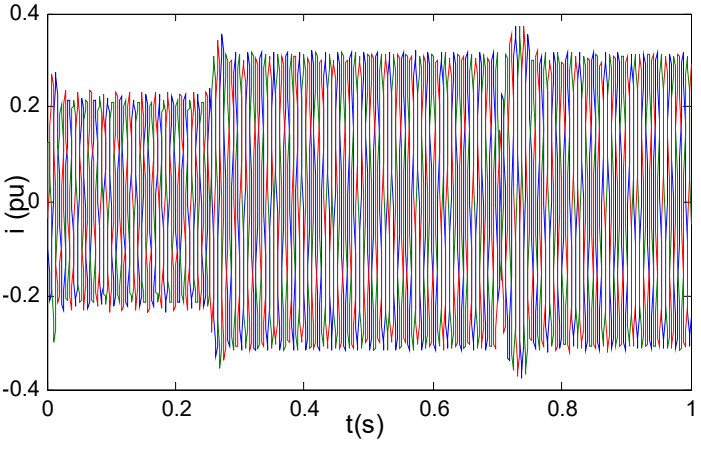


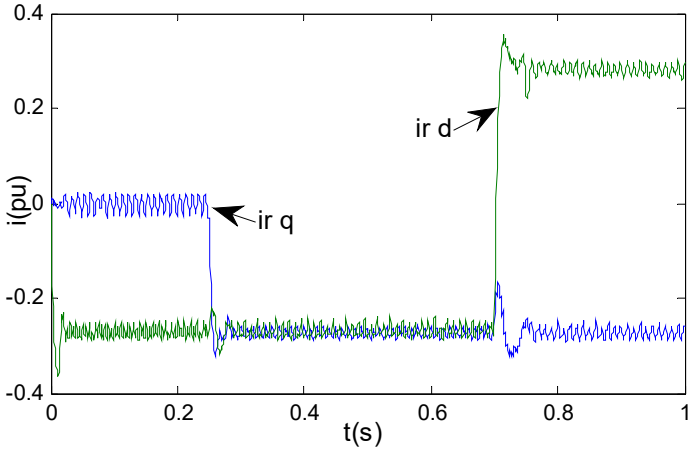
Figure 12 Sending end current (see online version for colours)





During simulation, the active power exchange between the series branch and the system is compensated by active power exchange of the parallel branch (Figures 9, 10 and 11). Sudden change in the current is observed (Figures 12 and 13).

Figure 13 Receiving end current (see online version for colours)



9 Fuzzy logic-based PI control structure

Fuzzy logic is a control technique based on degrees of truth to simulate human deductive of thinking; its main characteristic is the use of linguistic variables instead of the numerical ones in fuzzy logic conditional circumstances. It is intended as a rapprochement between the precision of the classical logic and the subtle imprecision of the real world.

The fuzzy logic regulator uses inferences with many rules based on linguistic variables (Bühler, 1994).

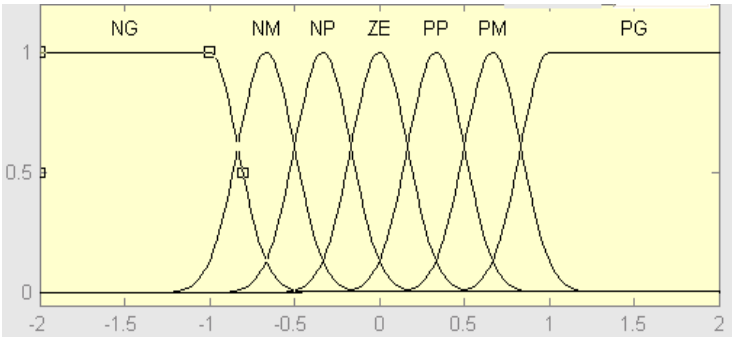
The basic configuration of a fuzzy logic controller is well defined in Bühler (1994). More sensitivity is provided by increasing the number of the rules (Bühler, 1994). In this application, a fuzzy logic-base PI controller is used, whose inputs are the error and the rate of error, to replace the conventional PI controller in the control circuits of the UPFC. The number of the membership function used in this application is seven and the system is formed of 49 rules.

The error signal is calculated from the difference between the output current of each converter (series and shunt converters) of the UPFC and the reference currents and the rate of error signal is calculated from the present error value and its previous one. The error signal and the rate of error signal are described as the fuzzy logic controller inputs; they are connected using Mamdani type inference method (Bühler, 1994).

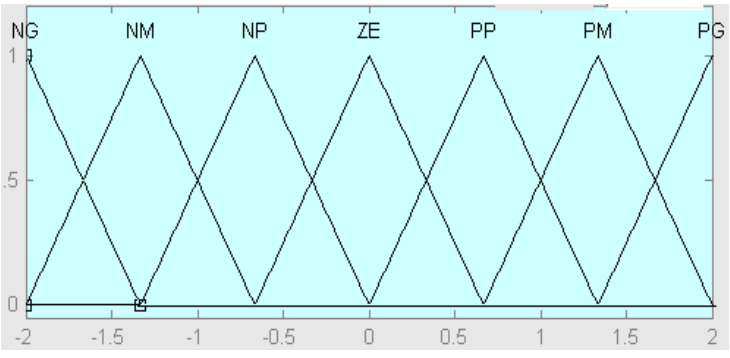
The membership functions for the input and the output used for fuzzy logic controller are represented in Figure 14(a) and Figure 14(b).

The decoupling strategy is performed by the rule-base matrix given by Table 2.

Figure 14 (a) Membership functions of error (b) Membership functions of change of error (see online version for colours)



(a)



(b)

Table 2 Representation of the inference rules

DE *E*	*NB*	*NM*	*NS*	*ZZ*	*PS*	*PM*	*PB*
PB	ZZ	PS	PM	PB	PB	PB	PB
PM	NS	ZZ	PS	PM	PB	PB	PB
PS	NM	NS	ZZ	PS	PM	PB	PB
ZZ	NB	NM	NS	ZZ	PS	PM	PB
NS	NB	NB	NM	NS	ZZ	PS	PM
NM	NB	NB	NB	NM	NS	ZZ	PS
NB	NB	NB	NB	NB	PM	NS	ZZ

10 Simulation results with use of fuzzy logic PI controller

The same simulation tests done in the case of conventional PI regulator was done with a fuzzy logic regulator to compare the robustness of the control strategy.

From the simulation results (Figures 15, 16 and 17), fuzzy PI controller has shown better regulating properties over the conventional PI controller. The proposed fuzzy PI controller tracks the active and reactive power reference setting more effectively with limited overshoots compared to conventional PI controller.

Figure 15 Sending end active and reactive power (see online version for colours)

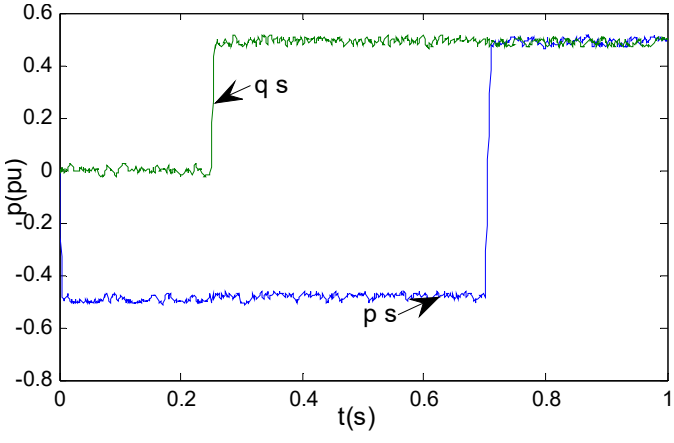


Figure 16 Sending end current (see online version for colours)

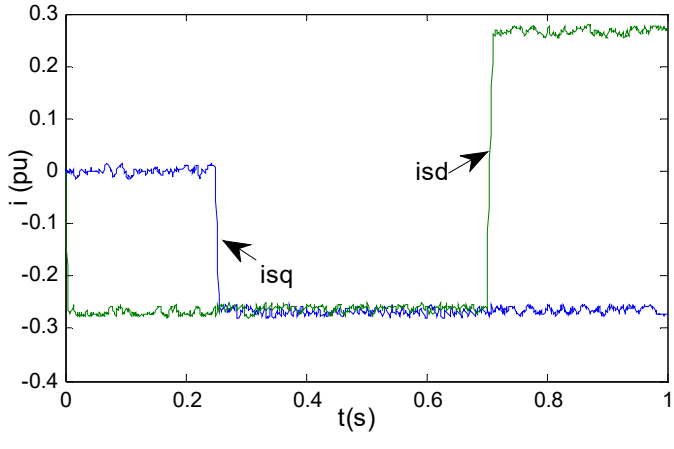
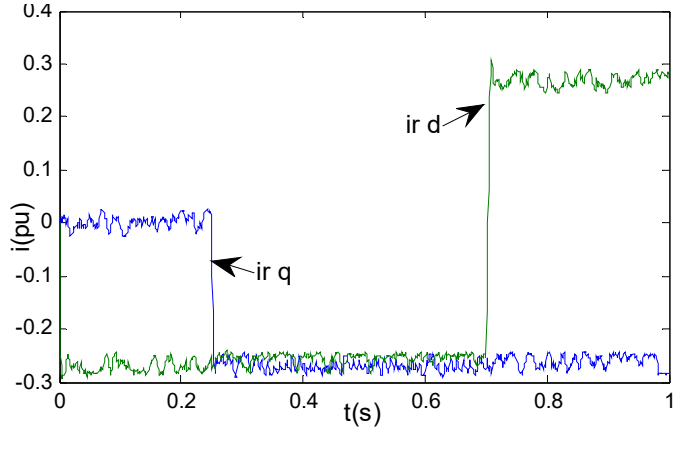


Figure 17 Receiving end current (see online version for colours)



11 Conclusions

This paper presents the application of the decoupled control strategy to regulate active and reactive powers independently in the event of changes in step points of the powers. Two types of controllers are used to handle the proposed control circuit: a conventional PI regulator and a fuzzy logic PI regulator.

From the simulation results, the fuzzy-PI controller has shown better regulating properties over the simple PI controller. The fuzzy-PI controller tracks the active and reactive power reference setting more effectively with limited overshoots compared to conventional PI controller.

Also, a three level NPC inverter is implemented in both series and shunt parts of the UPFC to get multi step voltage wave.

References

Berrahal, K., Bouhentala, A. and Bensalem, A. (2016) 'Reactive power compensation with five level based inverter', *Journal of Electrical Engineering*, Vol. 16, No. 4, pp.327–333.

Bouhali, O., François, B., Berkouk, E.M. and Sandemont, C.S. (2007) 'DC link capacitor in three-phas diode clamped inverter controlled by direct space vector of line-to-line voltages', *IEEE Trans. on Power Electronics*, Vol. 22, No. 5, pp.1636–1648.

Bühler, H. (1994) *Réglage par la logique floue*, Press Polytechinque et Universitaire Romandes, Lausanne.

Dai, K., Liu, P., Kang, Y. and Chen, J. (2001) 'Decoupling current control for voltage source converter in synchronous rotating frame', *4th IEEE International Conference on Power Electronics and Drive Systems, 2001*.

Farivar, G., Hredzak, B. and Agelidis, V.G. (2016) 'Decoupled control system for cascaded H-bridge multilevel converter based STATCOM', *IEEE Transactions on Industrial Electronics*, Vol. 63, No. 1, pp.322–331.

Fujita, H., Akagi, H. and Watanabe, Y. (2006) 'Dynamic control and performance of a unified power flow controller for stabilizing an ac transmission system', *IEEE Trans. Power Electron.*, July, Vol. 21, No. 4, pp.1013–1020.

Gholipour, E. and Saadate, S. (2005) 'Improving of transient stability of power systems using UPFC', *Transactions on Power Delivery*, April, IEEE, Part 2, Vol. 20, No. 2, pp.1677–1682.

Liu, L., Zhu, P., Kang, Y., Zhang, Y. and Chen, J. (2005) 'Control scheme and implementation of a unified power flow controller', *Proceedings of the Eighth International Conference on Electrical Machines and Systems*, Vol. 2, pp.1170–1175.

Naveena Bhargavi, R. (2013) 'A control approach for distributed power flow controller', *IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)*, Vol. 4, No. 2, pp.6–11, ISSN: 2278-1676.

Papic, I. (2000) 'UPFC model for stability calculations with decoupled Watt-Var control system', *10th Mediterranean Electrotechnical Conference, MeleCon*, May, Vol. 3.

Saribulut, L., Teke, A. and Tumay, M. (2011) 'Dynamic control of unified power flow controller under unbalanced network condition', *Simulation and Modeling Practice and Theory*, Vol. 19, No. 2, pp.817–836.

Taher, S.A., Akbari, S., Ketabi, A., Hematti, R. and Abdolalipour, A. (2009) 'Robust UPFC controller design using quantitative feedback theory method', *IEEE Bucharest Power Tech. Conference*, Bucharest, Romania, 28 June–2 July.

Ucar, M. and Ozdemir, E. (2008) 'Control of a 3-phase 4-leg active power filter under non-ideal mains voltage condition', *Electric Power System Research* Vol. 78, No. 1, pp.58–73.

Vural, A.M. and Tumay, M. (2007) 'Mathematical modeling and analysis of a unified power flow controller: a comparison of two approaches in power flow studies and effect of UPFC location', *Electrical Power and Energy Systems*, Vol. 29, No. 8, pp.617–629.

Xie, H., Mei, S., Gui, X., Liu, F. and Lu, Q. (2002) 'Multi-level controller design for UPFC', *Proc. Int. Conf. on Power System Technology Power Conf.*, Vol. 3, pp.1938–1942.

Yam, C.M. and Haque, M.H. (2004) 'ASVD based controller of UPFC power flow controller', *Electric Power System Research*, Vol. 70, No. 1, pp.76–84.

Zhang, Y., Liu, L., Zhu, P., Liu, X., Kang, Y. and Gao, Y. (2005) 'Double closed loop control and analysis for shunt inverter of UPFC', *Proceedings of the Eighth International Conference on Electrical Machines and Systems*, Vol. 2, pp.1118–1123.