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Lifelong Learning Programme

CMOS Analog Integrated Circuits

Part 4. Operational Amplifiers

Emil D. Manolov

Advanced level study programme in
Electronics Design and Integration Technologies

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4. Operational Amplifiers

CMOS Analog Integrated Circuits
(introductory course)

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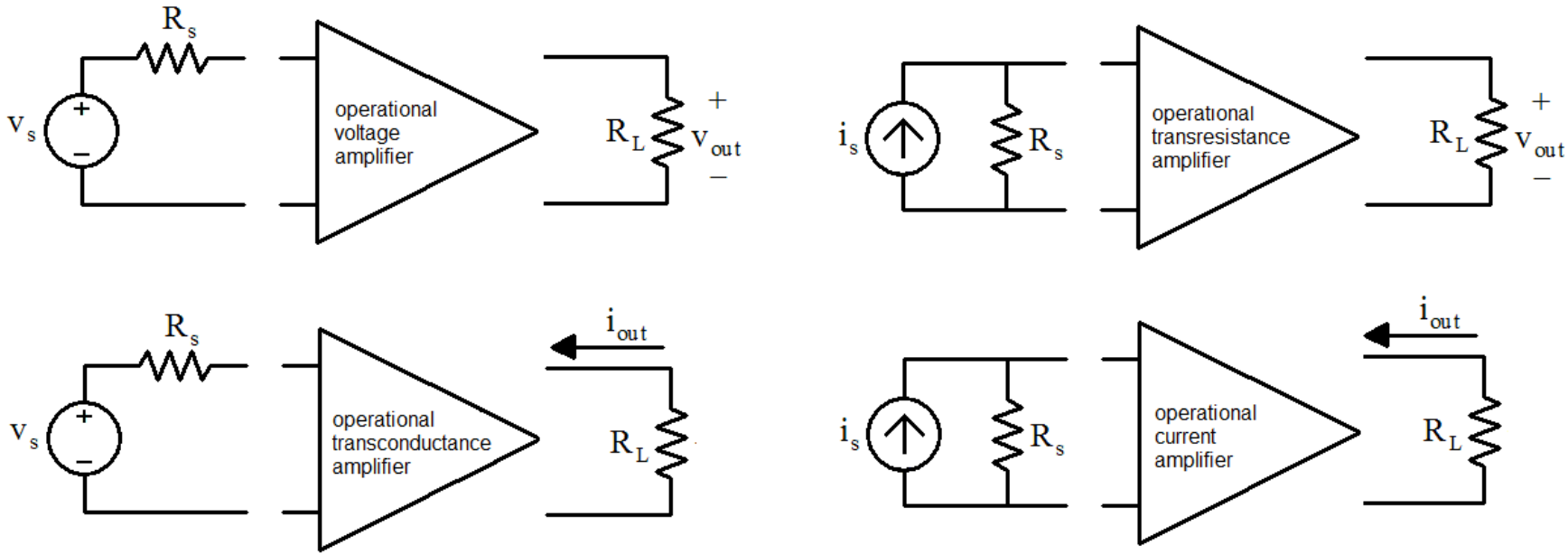
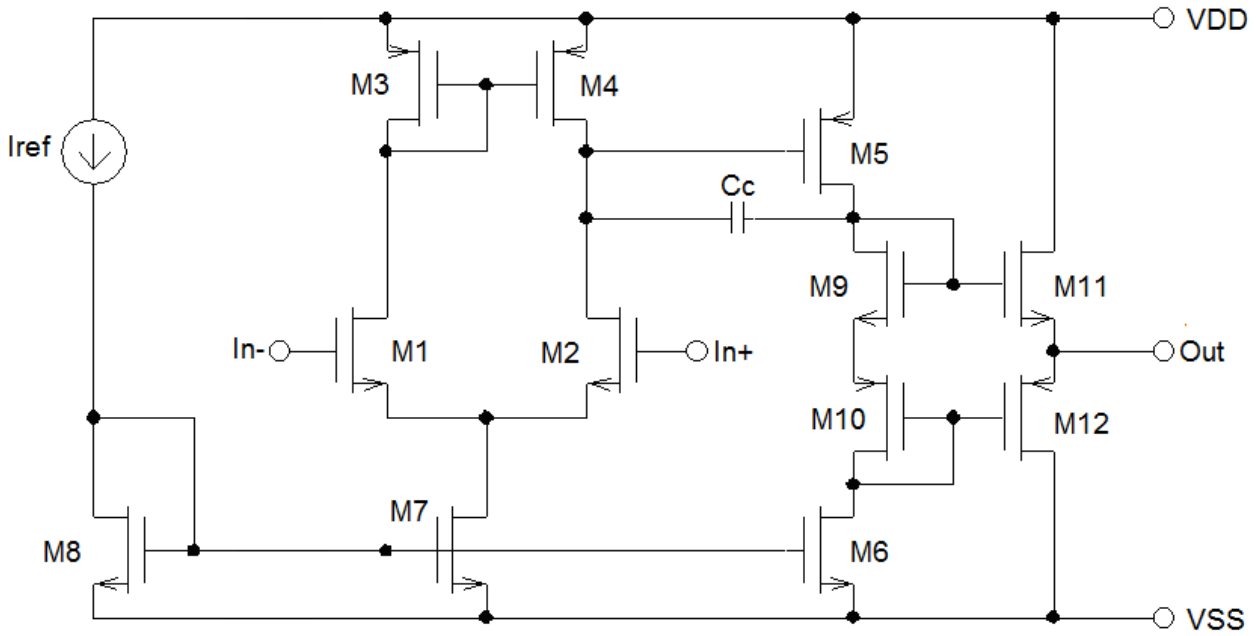
Operational amplifiers



Operational amplifiers are the most widely used block in the analog circuit design. Depending on the mode of representation of the signals (by current or voltage) four broad type of operational amplifiers are known:

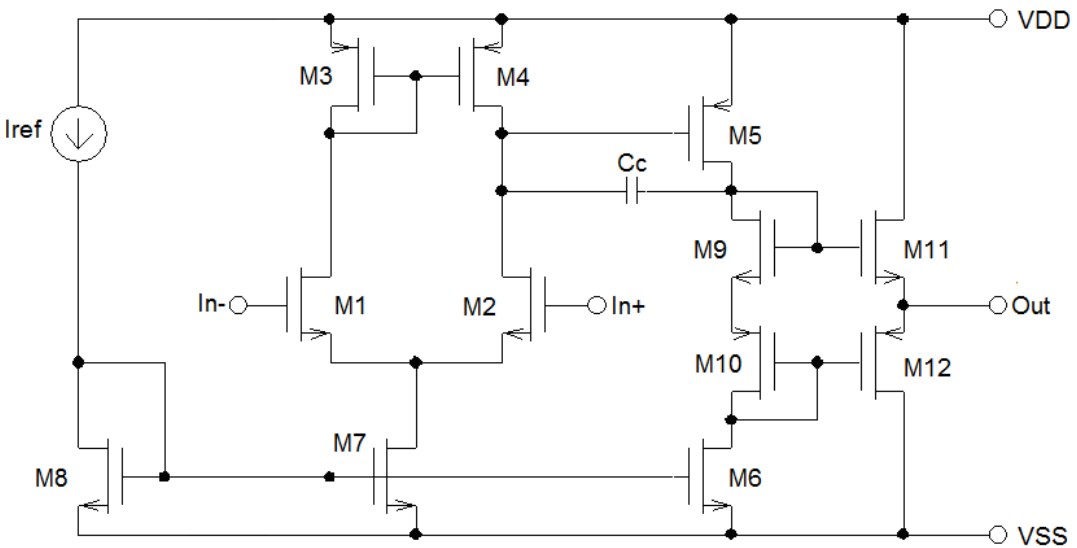
- operational voltage amplifier (usually called Op Amp): voltage input – voltage output;
- operational transconductance amplifier (OTA): voltage input – current output;
- operational transresistance amplifier (current mode amplifier, CMA): current input – voltage output;
- operational current amplifier (OCA): current input – current output.

Basic CMOS Operational Amplifier



The basic CMOS Op Amp configuration consists of two stages. The first stage is a differential amplifier (M1, M2, M7) with current mirror load (M3, M4). It ensures high value of the CMRR. The second stage is a class AB output amplifier with a complementary source-followers (M11,M12). M5 and M6 are common source amplifier with active load. Transistors M9 and M10 set the biasing of the output pair. The couples M8, M7 and M8,M6 are simple current mirrors. Iref is a constant current reference. As we know from previous modules, transistors M1 and M2, and M3 and M4 are identical. Miller capacitance Cc is the frequency compensation of the circuit.

Basic DC relations in the Op Amp



To obtain the basic DC relations in the Op Amp, the circuit is analyzed without exciting signal, i.e.

$$V(\mathrm{In}+) = V(\mathrm{In}-) = 0\mathrm{V}.$$

Thus

$$I_{ref} = I_{D8} = \frac{\mu_n C_{ox}}{2}\frac{W8}{L8}V_{eff\,8};$$

$$I_{D7} = \frac{W7/L7}{W8/L8}I_{D8} = \frac{W7/L7}{W8/L8}I_{ref};$$

Because of the symmetry in the input pair

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{D7}}{2} \quad \Rightarrow \quad \mu_n C_{ox}\frac{W1}{L1}V_{eff\,1} = \mu_p C_{ox}\frac{W3}{L3}V_{eff\,3}$$

To ensure the symmetrical load of the input diff amp, the next equations should be fulfilled

$$|V_{DS4}| = |V_{DS3}| = |V_{GS5}| \quad \Rightarrow \quad I_{D5} = I_{D3}\frac{W5/L5}{W3/L3} = \frac{I_{D7}}{2}\frac{W5/L5}{W3/L3} = \frac{I_{ref}}{2}\frac{W5/L5}{W3/L3}\frac{W7/L7}{W8/L8}.$$

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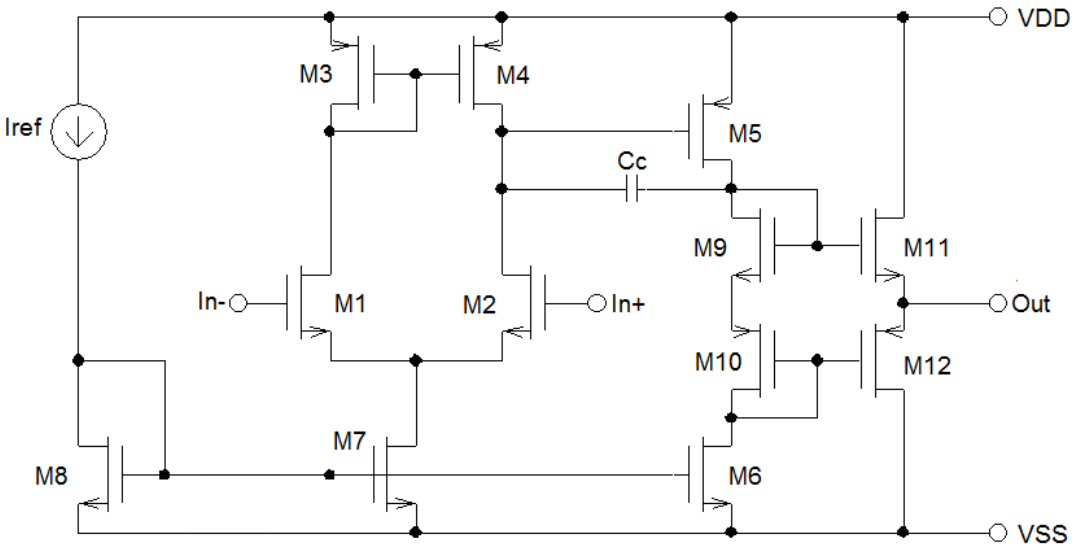
Basic DC relations in the Op Amp (cont.)



Using the basic property of the current mirror we can find

$$I_{D6} = I_{ref}\frac{W6/L6}{W8/L8}.$$

Because of currents ID5 and ID6 are equals

$$I_{D5} = I_{D6} = I_{D9} = I_{D10};$$

$$\frac{I_{ref}}{2}\frac{W5/L5}{W3/L3}\frac{W7/L7}{W8/L8} = I_{ref}\frac{W6/L6}{W8/L8}$$

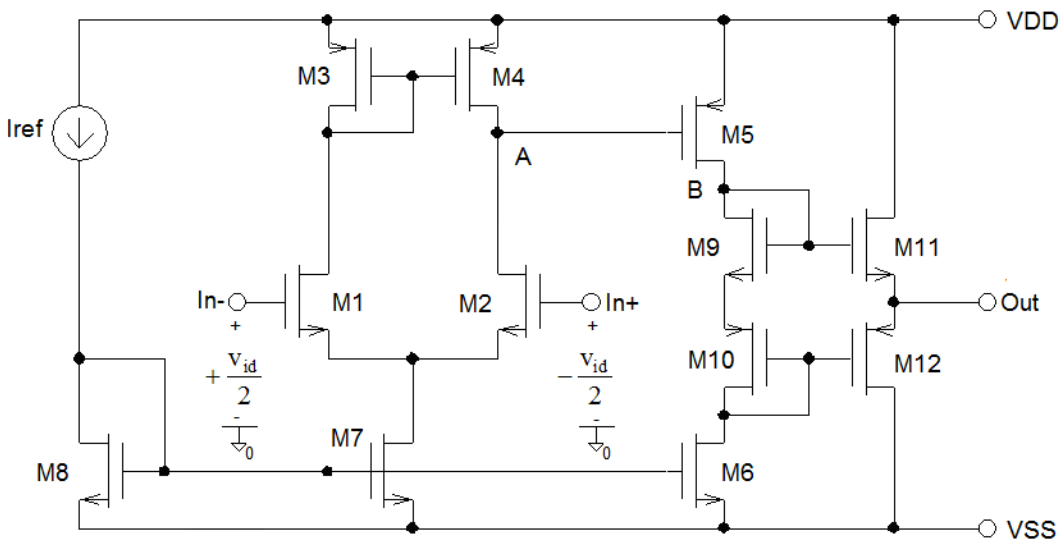
and finally $\frac{W5}{L5}\frac{W7}{L7} = 2\frac{W6}{L6}\frac{W3}{L3}$, which is the condition for normally operation of the circuit.

To assure the desired biasing of the output pair, the transistors M9 and M10 should be sized using the following formulas

$$\frac{L9}{W9} = \frac{2\cdot I_{D5}}{\mu_n C_{ox} V_{eff\,9}^2}; \quad \frac{L10}{W10} = \frac{2\cdot I_{D5}}{\mu_p C_{ox} V_{eff\,10}^2};$$

$$I_{D11} = I_{D12} = I_{D6}\frac{W12/L12}{W10/L10} = I_{D6}\frac{W11/L11}{W9/L9}.$$

Low-frequency analysis of Op Amp



The formulas for voltage gain **Au** and output resistance $\mathbf{r_{out}}$ of the OP Amp can be obtained by using the equations for the simple amplifying stages, given in Module 3. Hence, the signals at point A and B are as follow

$$v_A = A_{u1} v_{id} = \frac{g_{m2}}{g_{o2} + g_{o4}} v_{id} \text{ and}$$

$$v_B = A_{u2} v_A = \frac{-g_{m5}}{g_{o5} + g_{o6}} v_A$$

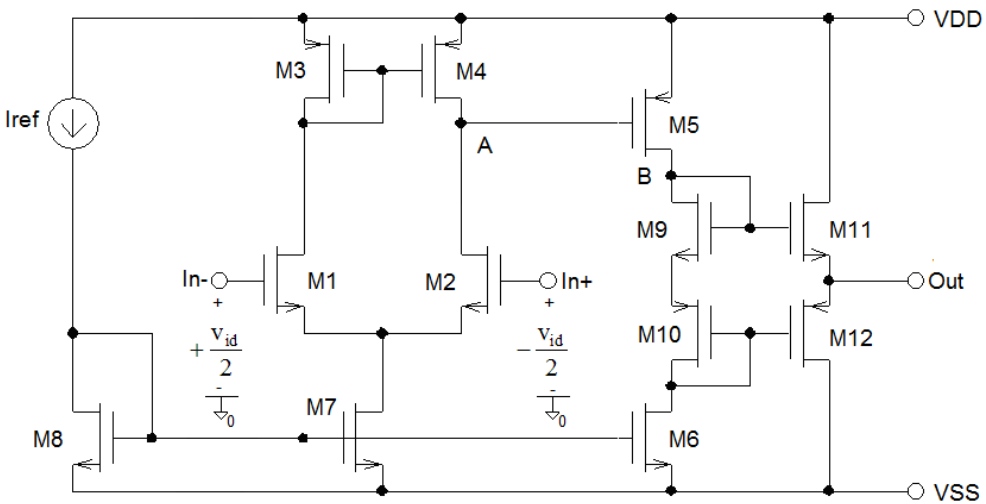
The final results are $A_u = A_{u1} A_{u2} = \frac{v_{out}}{v_{id}} \approx \frac{v_B}{v_{id}} = \frac{-g_{m2}\, g_{m5}}{(g_{o2} + g_{o4})(g_{o5} + g_{o6})}$ and $r_{out} = \frac{1}{g_{m11} + g_{m12}}$,

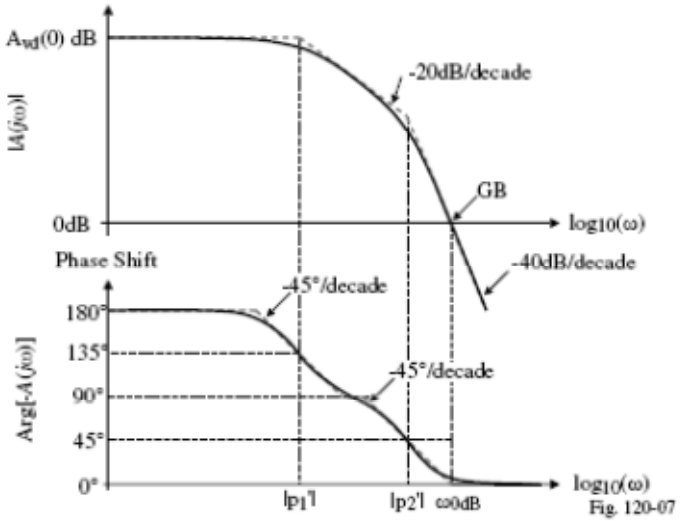
where

$$g_{m2} = \sqrt{2\mu_n C_{ox} \frac{W2}{L2} I_{d2}} = \mu_n C_{ox} V_{eff\,2} = \frac{2I_{D2}}{V_{eff\,2}}; \quad g_{m5} = \sqrt{2\mu_p C_{ox} \frac{W5}{L5} I_{d5}} = \mu_p C_{ox} V_{eff\,5} = \frac{2I_{D5}}{V_{eff\,5}}$$

$$g_{o2} = \lambda_{n2} I_{D2}; \quad g_{o4} = \lambda_{p4} I_{D2}; \quad g_{o5} = \lambda_{p5} I_{D5}; \quad g_{o6} = \lambda_{n6} I_{D5}.$$

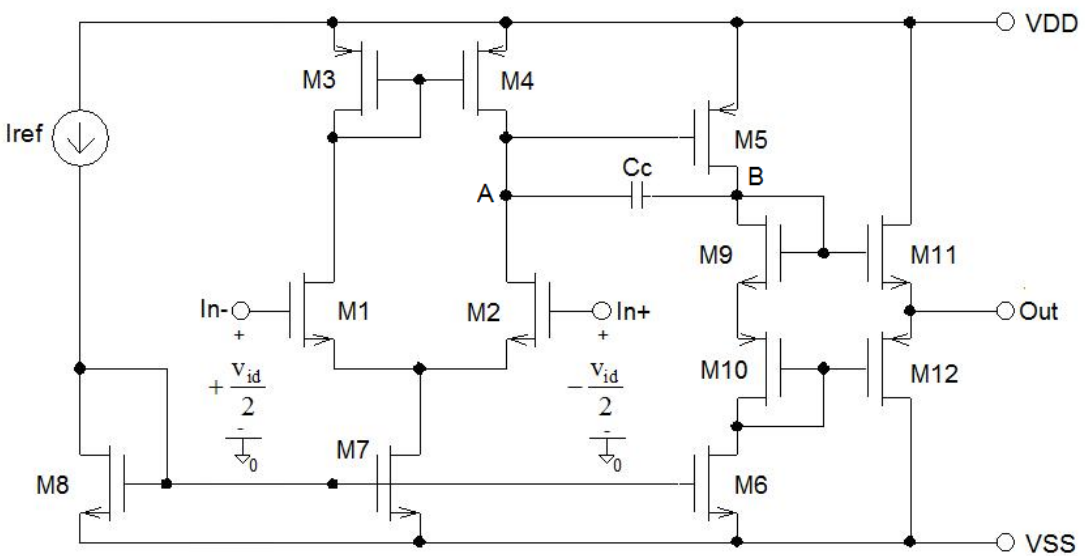
High-frequency behavior of Op Amp

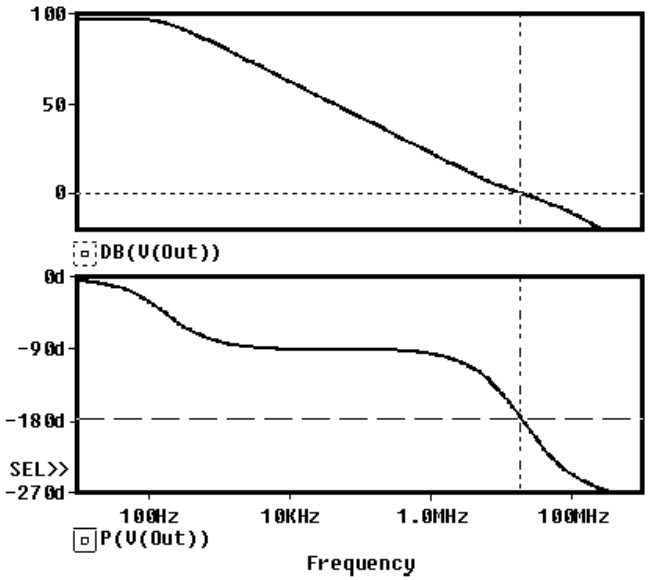




The discussed circuit has the disadvantage of having two high-impedance nodes in points A and B. This implies that two poles will be dominant, which deteriorate the phase margin of the Op Amp. The right graphic shows the open loop uncompensated frequency response of the amplifier. There are two poles in the circuit and at the point at which the open-loop gain is unity (0 dB) corresponds the phase shift is higher than 180 degree. As we know the maximum admissible phase shift is 135 degree, which assures a phase margin of 45 degree. Otherwise the circuit is highly unstable, as it is in our case. To avoid the instability the frequency compensation is used, which guarantees a phase margin no less than a 45 degree. (Frequently, 60 degree is desired for better safety).

Frequency compensation of Op Amp





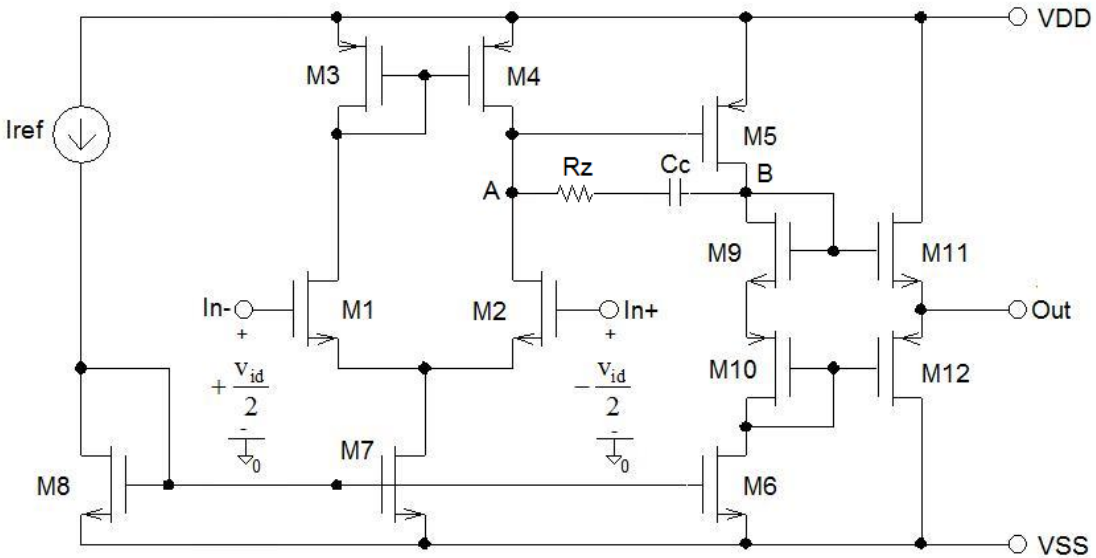
To compensate the Op Amp the capacitor **Cc** is used. In this way the dominant pole is translated towards the low frequencies. The next formula can be used for calculation the value of the capacitor **Cc**.

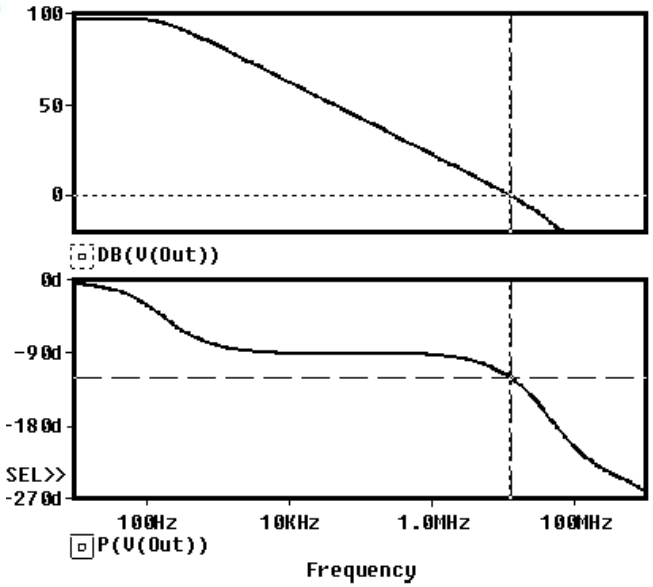
$$f_u \approx GBW = A_u BW \approx A_{u1}A_{u2}\frac{g_{02}+g_{o4}}{2\pi A_{u2}C_c} = A_{u1}\frac{g_{02}+g_{o4}}{2\pi C_c} = \frac{g_{m2}}{g_{o2}+g_{o4}}\frac{g_{02}+g_{o4}}{2\pi C_c} = \frac{g_{m2}}{2\pi C_c}$$

In this formula, **fu** is the frequency, at which the open-loop gain is unity (usually is known as unity-gain frequency). The value of **fu** is very close to the gain-bandwidth product, **GBW**.

But the results shown in the right graphics demonstrate that despite of applied compensation the Op Amp is unstable again. An additional right-hand plane zero appears, which boosts the magnitude while decreasing the phase.

Zero compensation of Op Amp





As we seen in the previous slide, when the compensation capacitor is included, the right-hand plane zero appears. Its value is given by $z = g_{m5}/C_c$. To eliminate the problem a resistor in series with the compensation capacitor can be included. Then the formula for zero changes

$$z = \left[C_c \left(\frac{1}{g_{m5}} - R_z \right) \right]^{-1}.$$

If **Rz** is selected equal to $\mathbf{1/g_{m5}}$ the zero disappears. If **Rz** is larger than $\mathbf{1/g_{m5}}$ the phase margin increases. In the discussed case the result is extremely positive. The using of zero nulling resistor increases the phase margin up to 60 degree.

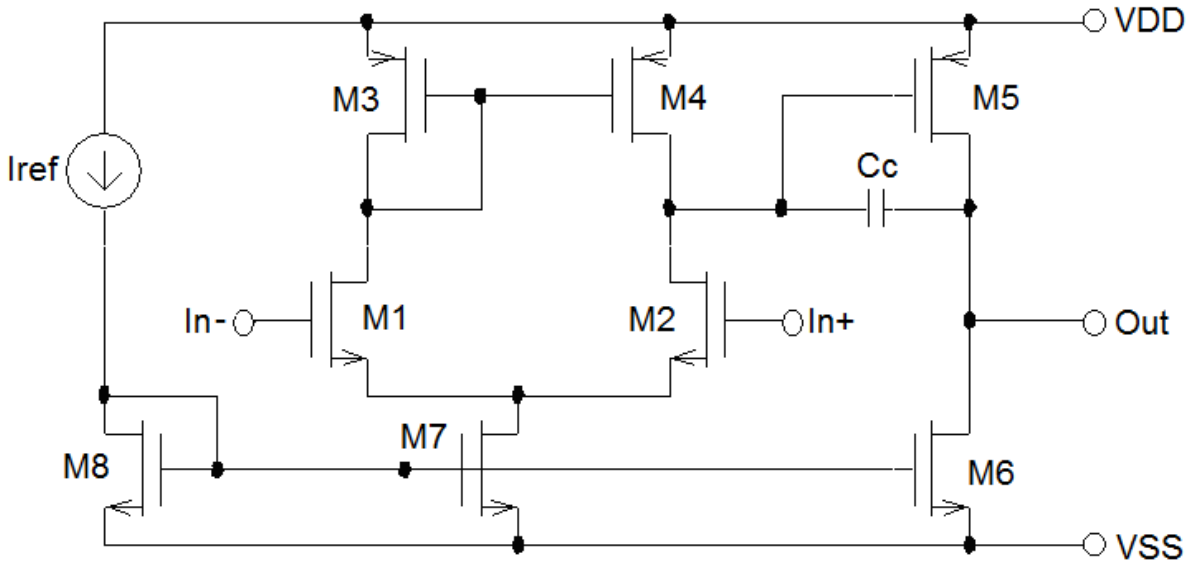
Operational transconductance amplifiers (OTAs)

The operational transconductance amplifiers find wide application in the analog integrated circuit design. Because of high input impedance of the MOS devices the condition for low-output impedance is not actual for the amplifiers which are inside integrated circuit. In this case only capacitive load presents at the output and consequently high-impedance output stage with high voltage gain is suitable to use.

There are tree popular types of CMOS OTA circuit architectures:

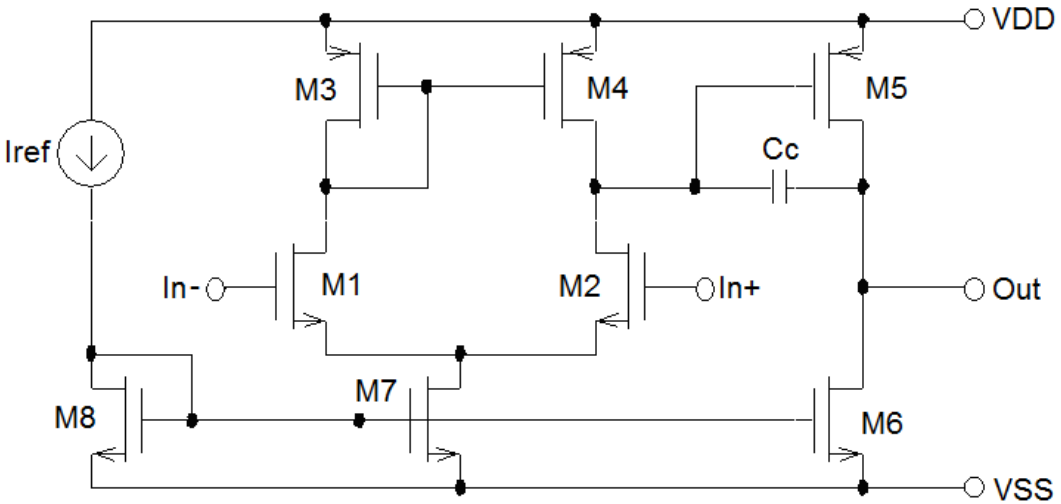
- Two stage OTA (most frequently known as Miller OTA);
- Cascode OTA;
- Folded-cascode OTA.

Miller OTA



The Miller OTA architecture consists of two stages. Its configuration is similar to the considered operational voltage amplifier Op Amp. The first stage is a differential amplifier (M1, M2, M7) with current mirror load (M3, M4). It ensures high value of the CMRR. The second stage is a common source amplifier with active load (M5, M6). Transistor M8 is for the biasing of M8-M7 and M8-M6 current mirrors. Iref is a constant current reference. As we know from previous modules, transistors M1 and M2, and M3 and M4 are identical. Also the Miller capacitance Cc is introduced, in order to guarantee the stability of the circuit.

Basic DC relations in Miller OTA



To obtain the basic DC relations in the Miller OTA the circuit is analyzed without exciting signal, i.e. Vin+=Vin-=0V.

Thus

$$I_{ref} = I_{D8} = \frac{\mu_n C_{ox}}{2}\frac{W8}{L8}V_{eff\,8};$$

$$I_{D7} = \frac{W7/L7}{W8/L8}I_{D8} = \frac{W7/L7}{W8/L8}I_{ref}.$$

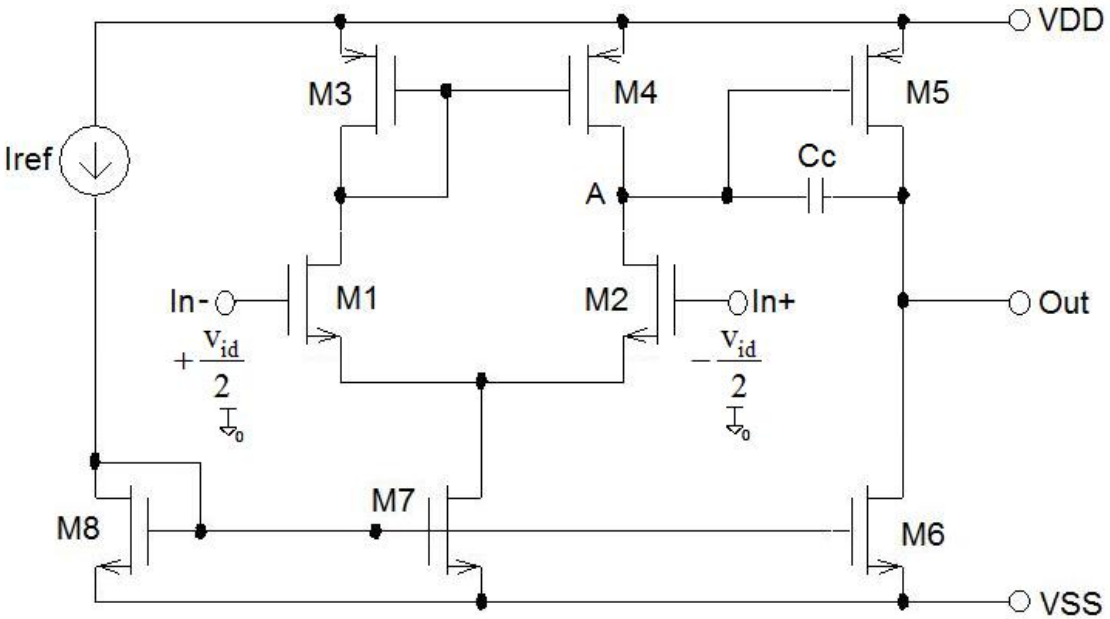
$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{D7}}{2} \quad \Rightarrow \quad \mu_n C_{ox}\frac{W1}{L1}V_{eff\,1} = \mu_p C_{ox}\frac{W3}{L3}V_{eff\,3}$$

To ensure the symmetry of the input diff amp, the following equations could be fulfilled

$$|V_{DS4}| = |V_{DS3}| = |V_{GS5}| \quad \Rightarrow \quad I_{D5} = I_{D3}\frac{W5/L5}{W3/L3} = \frac{I_{D7}}{2}\frac{W5/L5}{W3/L3} = \frac{I_{ref}}{2}\frac{W5/L5}{W3/L3}\frac{W7/L7}{W8/L8};$$

$$I_{D6} = I_{ref}\frac{W6/L6}{W8/L8}; \quad I_{D5} = I_{D6} \Rightarrow \quad \frac{I_{ref}}{2}\frac{W5/L5}{W3/L3}\frac{W7/L7}{W8/L8} = I_{ref}\frac{W6/L6}{W8/L8} \Rightarrow \quad \frac{W5}{L5}\frac{W7}{L7} = 2\frac{W6}{L6}\frac{W3}{L3}.$$

AC analysis of Miller OTA



The formulas for the low-frequency parameters of the Miller OTA are similar to the formulas for Op Amp. Hence, the transconductance **Gm** and the output resistance $\mathbf{r_{out}}$ are

$$G_m = \frac{i_o}{v_{id}} = \frac{g_{m5} \cdot g_{m2}}{g_{o2} + g_{o4}};$$

$$r_{out} = \frac{1}{g_{o5} + g_{o6}}.$$

The voltage gain of the amplifier is

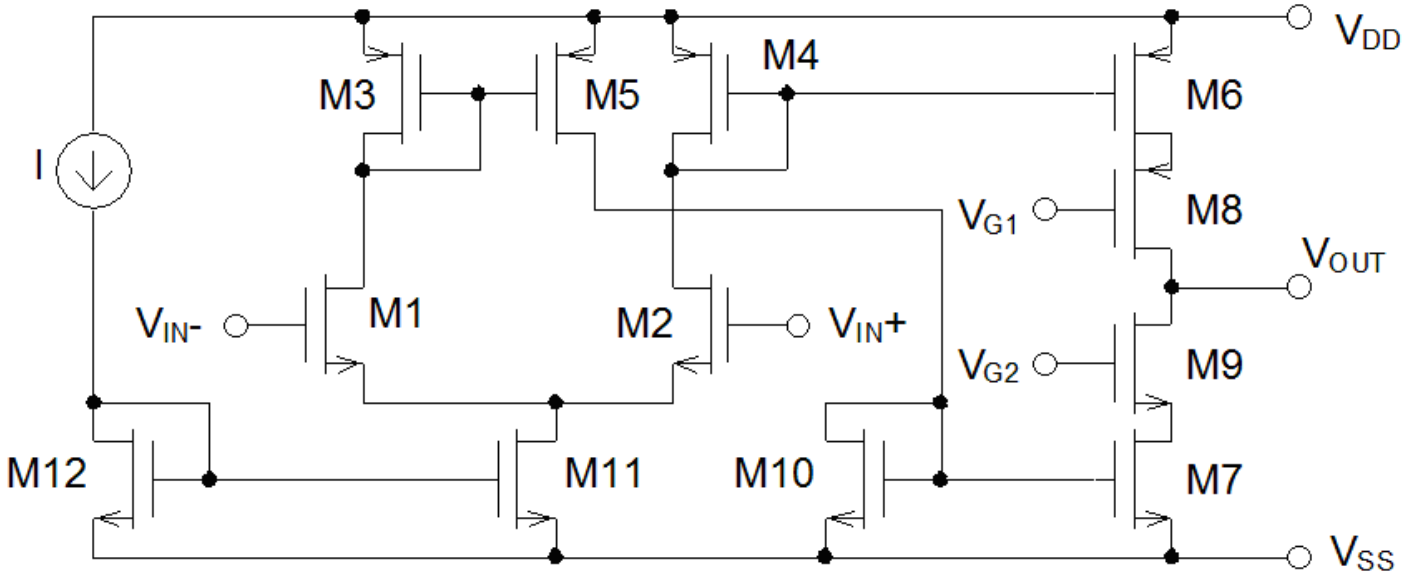
$$A_u = \frac{v_{out}}{v_{id}} = \frac{i_o r_{out}}{v_{id}} = \frac{i_o}{v_{id}} r_{out} = G_m r_{out} = \frac{g_{m5} \cdot g_{m2}}{(g_{o5} + g_{o6})(g_{o2} + g_{o4})}.$$

The gain-bandwidth product and the slew rate depend on the value of the capacitance Cc:

$$GBW = \frac{g_{m1}}{2\pi C_c}; \quad SR = \frac{I}{C_c}, \text{ where } I = \min(I_{D5}, I_{D7}).$$

In most cases the using of nulling resistor is imperativeness. Thus $R_z = 1/g_{m5}$.

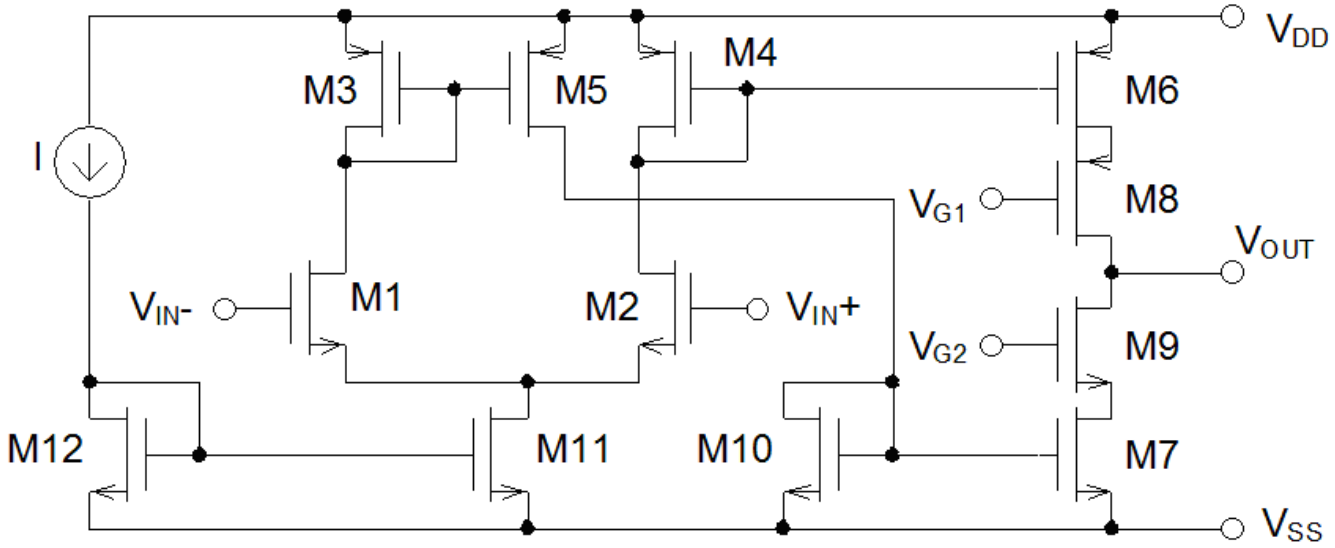
Cascode OTA



The figure shows the second type OTA configuration – **cascode OTA**. The input differential pair (M1, M2, M11) has as load transistors M3 and M4, connected as active resistances. The currents of the diff amp are transferred to the output push-pull cascode (M7-M9 and M6-M8) by using M3-M5, M10-M7 and M4-M6 current mirrors.

The most important advantage of this circuit is the present of only one high-impedance node, which is at the output. The frequency behavior of cascode OTA depends on the capacitor **CL** connected from the output to the ground. When the value of **CL** increases and the compensation increases, which keep the op amp stable for a large values of the capacitor.

Cascode OTA – basic DC relations

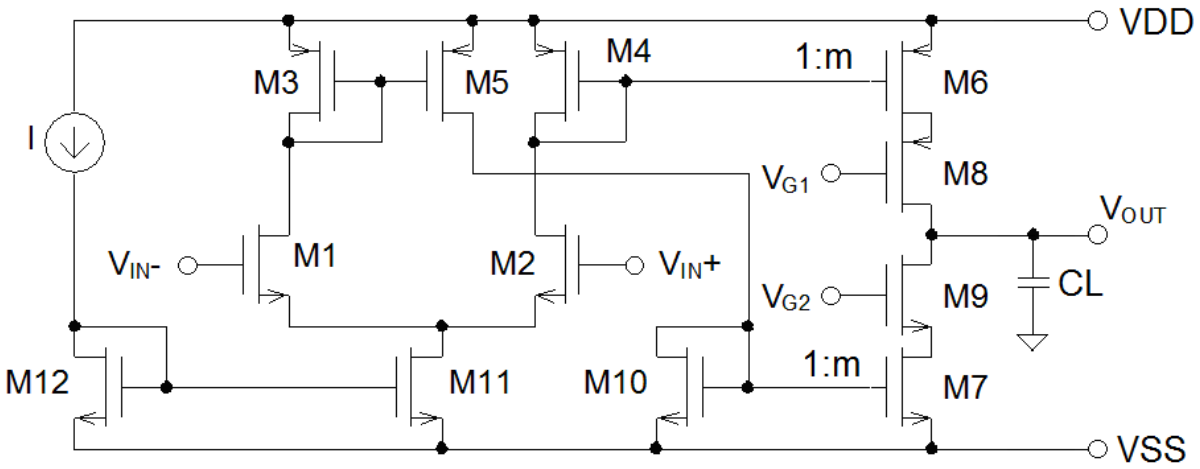


The DC analysis of the circuit is made in the condition that Vin-=Vin+= 0V and that all transistors operates in saturation. To keep the symmetry in the circuit, M1 and M2 are equals, as well as M3, M4 and M5. The transistors in the couples M7-M9 and M6-M8 are equals too. Then, the basic relation are

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5} = I_{D10} = \frac{I_{D11}}{2} = \frac{Iss}{2}; \quad I_{D6} = I_{D8} = I_{D9} = I_{D7} = \frac{W7/L7}{W10/L10} I_{D1} = \frac{W6/L6}{W4/L4} I_{D2};$$

$$I_{D11} = \frac{W11/L11}{W12/L12} I = Iss; \quad \mu_p C_{ox} \frac{W3}{L3} V_{eff\,3} = \mu_n C_{ox} \frac{W10}{L10} V_{eff\,10}; \quad \mu_p C_{ox} \frac{W6}{L6} V_{eff\,3} = \mu_n C_{ox} \frac{W7}{L7} V_{eff\,10}.$$

Cascode OTA – basic AC relations



$$I_{D11} = \frac{W11/L11}{W12/L12} I = Iss$$

$$\frac{W6/L6}{W4/L4} = \frac{W7/L7}{W10/L10} = m$$

Let a small differential signal **Vid** is applied to the inputs of the OTA (Vin-=Vid/2 and Vin+=-Vid/2). This signal provokes the appearance of a small ac component **i** in the currents of the OTA.

$$i = g_{m1}\frac{v_{id}}{2}; \quad I_{D1} = I_{D3} = I_{D5} = I_{D10} = \frac{Iss}{2} + i; \quad I_{D2} = I_{D4} = I_{D5} = \frac{Iss}{2} - i;$$

$$I_{D6} = I_{D8} = mI_{D2} = m\left(\frac{Iss}{2} - i\right); \quad I_{D7} = I_{D9} = mI_{D1} = m\left(\frac{Iss}{2} + i\right);$$

$$i_{out} = I_{D8} - I_{D9} = m\left(\frac{Iss}{2} - i\right) - m\left(\frac{Iss}{2} + i\right) = 2mi = 2mg_{m1}\frac{v_{id}}{2} = mg_{m1}v_{id};$$

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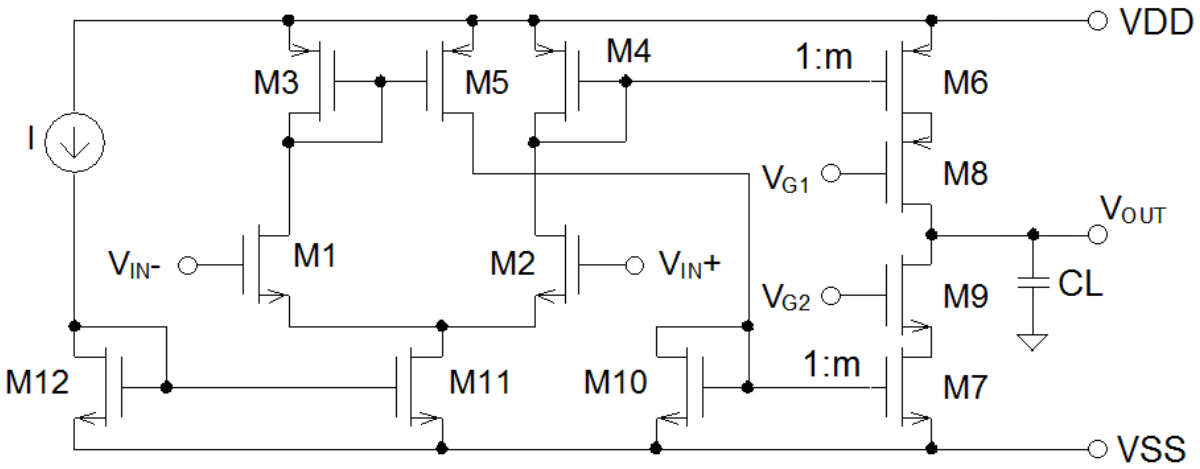
Cascode OTA – basic AC relations (cont.)



$$I_{D11} = \frac{W11/L11}{W12/L12} I = Iss$$

$$\frac{W6/L6}{W4/L4} = \frac{W7/L7}{W10/L10} = m$$

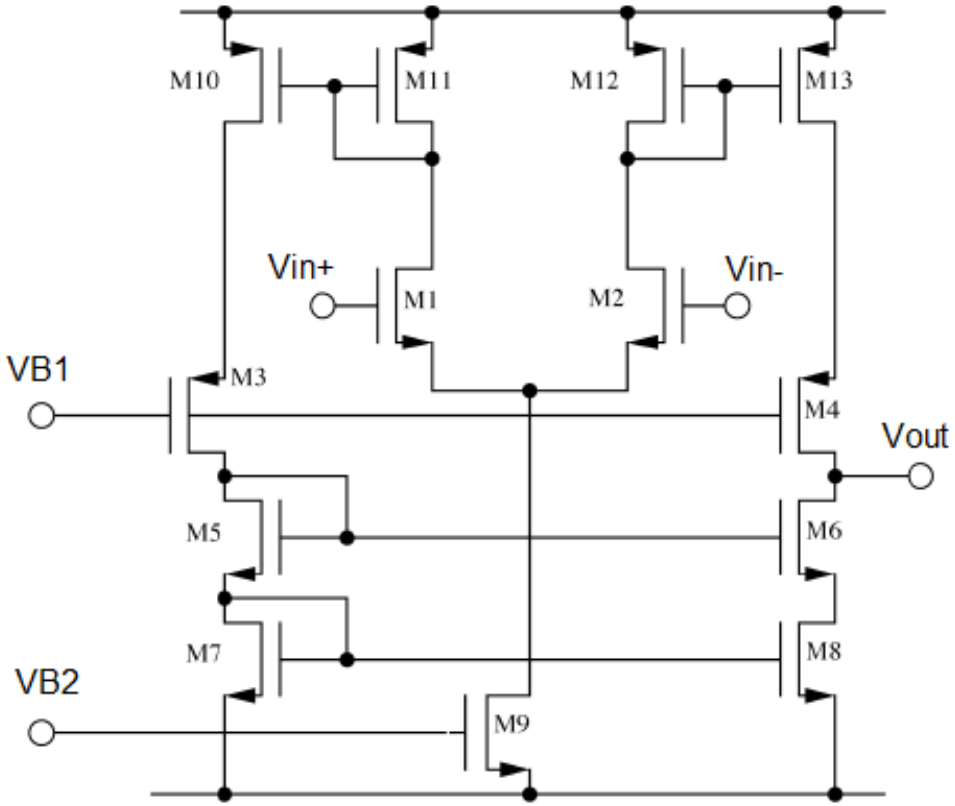
Finally, the formulas for the basin AC parameters of the cascode OTA are

$$G_m = \frac{i_{out}}{v_{id}} = m \cdot g_{m1}; \quad r_{out} = \frac{1}{g_{o9-7} + g_{o8-6}} = \frac{1}{g_{m9} r_{o7} r_{o9} + g_{m8} r_{o6} r_{o8}};$$

$$Au = G_m r_{out}; \quad BW = f_{(-3dB)} = \frac{1}{2\pi r_{out} C_L}; \quad GBW = Au \cdot BW = \frac{m \cdot g_{m1}}{2\pi C_L};$$

$$SR = \frac{m \cdot Iss}{C_L} = \frac{m}{C_L} \frac{W11/L11}{W12/L12} I$$

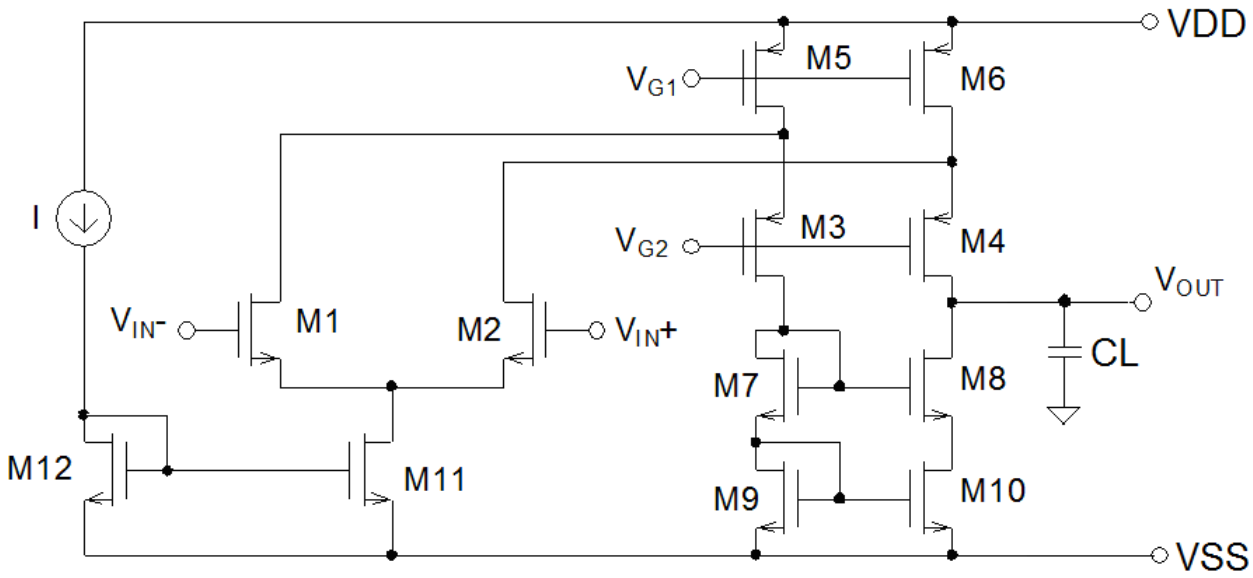
Practical implementation of cascode OTA



One practical implementation of the cascode OTA is shown of the figure. The main advantage of this circuit is its symmetry. The input devices have exactly the same DC voltage and load impedance. The output configuration is with maximum symmetry, also. As a result, matching is improved, which provides better offset and CMRR specifications.

The basic parameters of the circuit are identical to the presented in the previous slides.

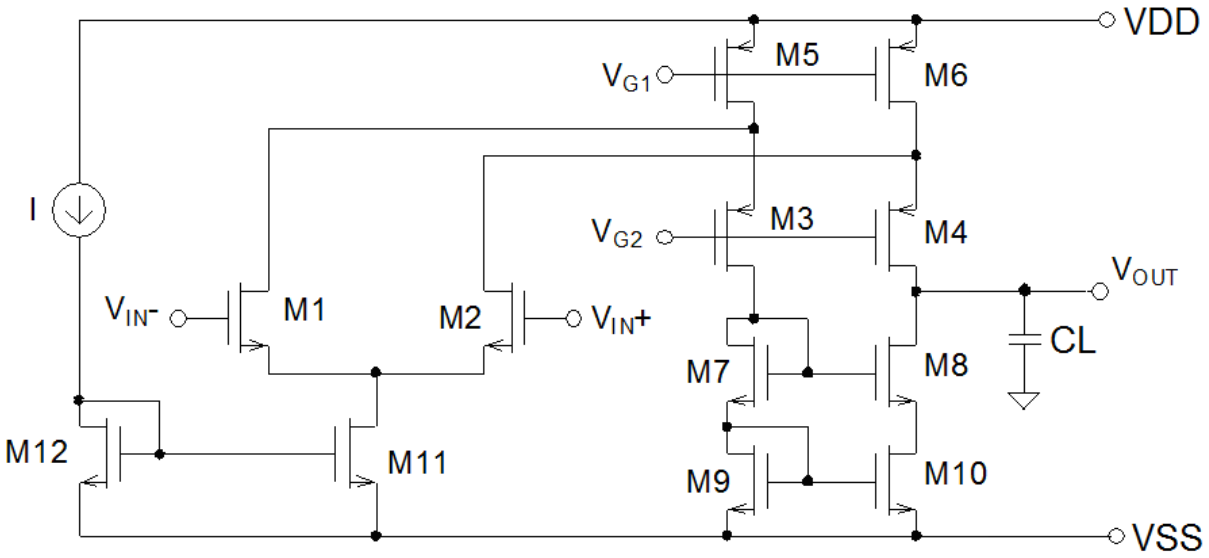
Folded cascode OTA



The figure shows the third basic type OTA configuration – **folded cascode OTA**. The input differential pair consists of transistors M1, M2 and M11. The transistors M1, M5 and M3 (M2, M6 and M4) form two folded cascode amplifiers. Transistors M5 and M6 are DC current sources for biasing of the stages. Transistors M3 and M4 are connected in common gate configuration and have a very small input resistance (1/gm). The cascode current mirror (M7, M8, M9,M10), which is the load of the amplifiers, transforms the differential signals at the drains of the M3 and M4 in single-ended output signal.

As a previous discussed cascode OTA, the folded cascode OTA has only one high-impedance node, which is at the output. Therefore the frequency compensation is simplified and is accomplished with the load capacitor **CL** connected from the output to the ground.

Folded cascode OTA – basic DC relations

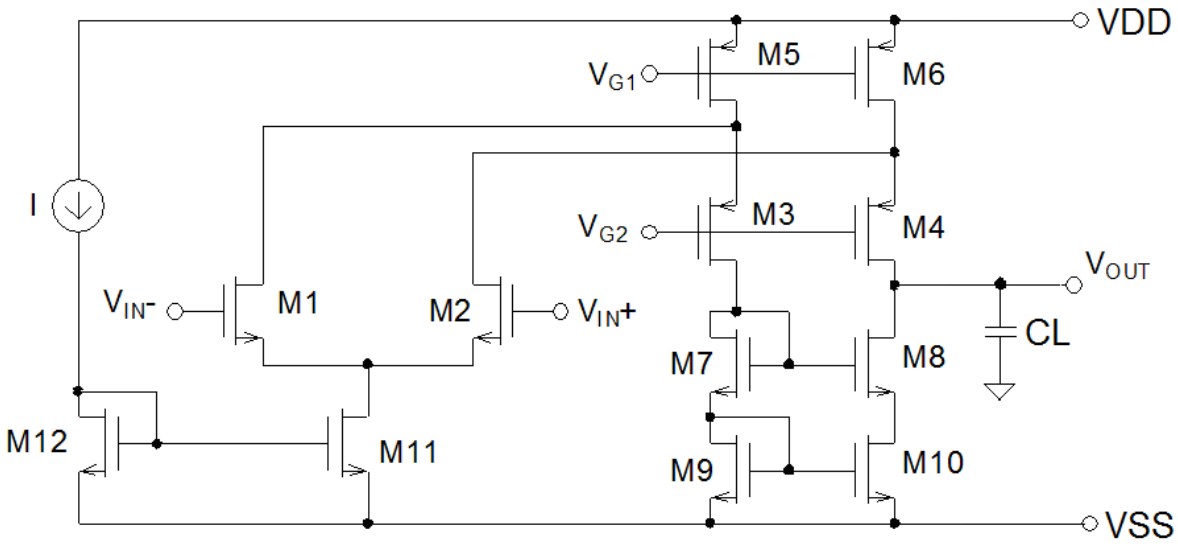


The relations between the currents in the circuit are obtained in the condition that both inputs are grounded and that all transistors operates in saturation. Because of the symmetry in the circuit, M1 and M2 are equals, as well as M5 and M6, M3 and M4, M7 and M8, and M9 and M10. Then

$$I_{D11} = \frac{W11/L11}{W12/L12} I = Iss; \quad I_{D1} = I_{D2} = \frac{Iss}{2}; \quad I_{D5} = I_{D6} = Idd \geq Iss;$$

$$I_{D3} = I_{D7} = I_{D9} = I_{D4} = I_{D8} = I_{D10} = Idd - \frac{Iss}{2}$$

Folded cascode OTA – basic AC relations



Let a small differential signal **Vid** is applied to the inputs of the OTA (Vin-=Vid/2 and Vin+=-Vid/2). This signal provokes the appearance of a small ac component **i** in the currents:

$$i = g_{m1}\frac{v_{id}}{2}.$$

$$I_{D1} = \frac{Iss}{2} + i; \quad I_{D2} = \frac{Iss}{2} - i; \quad I_{D3} = I_{D5} - I_{D1} = Idd - \left(\frac{Iss}{2} + i\right); \quad I_{D4} = I_{D6} - I_{D2} = Idd - \left(\frac{Iss}{2} - i\right);$$

$$I_{D3} = I_{D7} = I_{D9} = I_{D10} = I_{D8}; \quad i_{out} = I_{D4} - I_{D8} = 2i = 2g_{m1}\frac{v_{id}}{2} = g_{m1}v_{id}; \quad G_m = \frac{i_{out}}{v_{id}} = g_{m1};$$

$$r_{out} = \frac{1}{g_{o8-10} + g_{o4-6-2}}; \quad g_{o8-10} = \frac{g_{o8}g_{o10}}{g_{m8}}; \quad g_{o4-6-2} = \frac{g_{o4}\left(g_{o6} + g_{o2}\right)}{g_{m4} + g_{mb4}}; \quad Au = G_m r_{out};$$

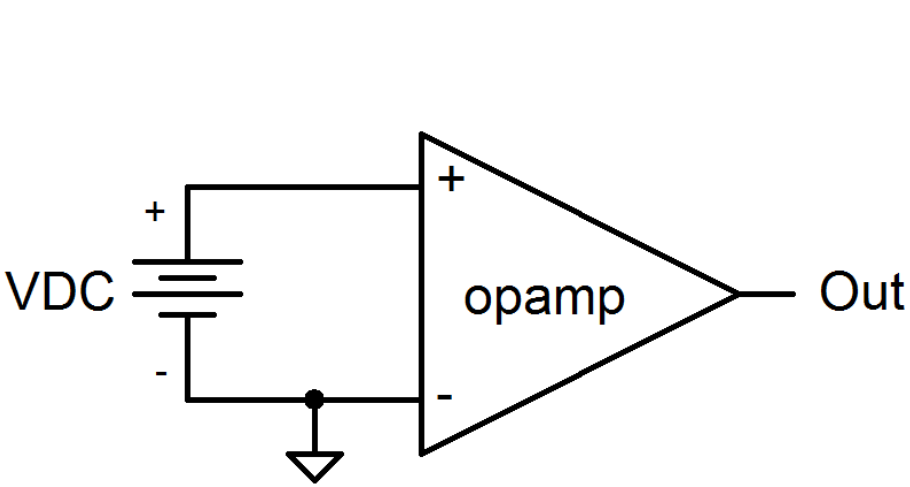
$$BW = f_{(-3dB)} = \frac{1}{2\pi r_{out} C_L}; \quad GBW = Au \cdot BW = \frac{g_{m1}}{2\pi C_L}; \quad SR = \frac{Idd}{C_L}.$$

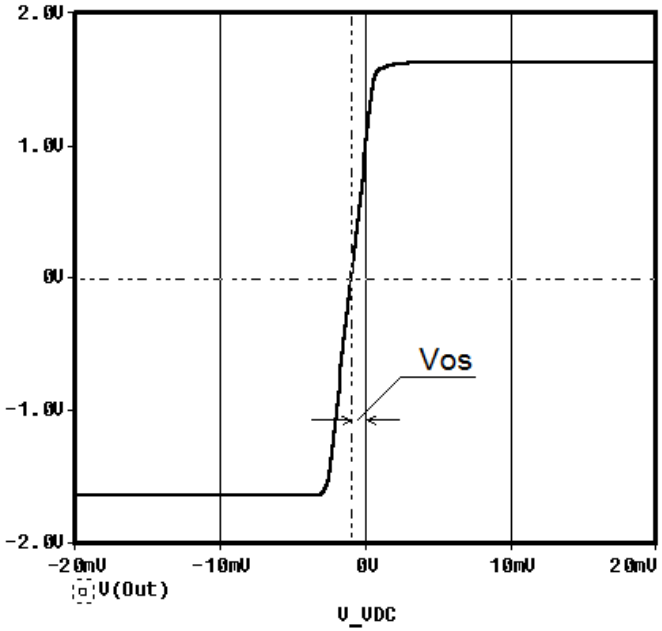
Test circuits for operational amplifiers simulation

The problem for simulation testing of basic parameter and characteristics of the operational amplifiers is extremely important for the successful design of an analog integrated circuit. Because of the contemporary methods for simulation are very precise and reliably, the using of simulations allows to estimate the performance of the designed circuit before implementation and in this way to avoid the faults and defects in the prototype.

The most convenient approaches to simulation testing of the operational amplifiers will be presented in the next slides.

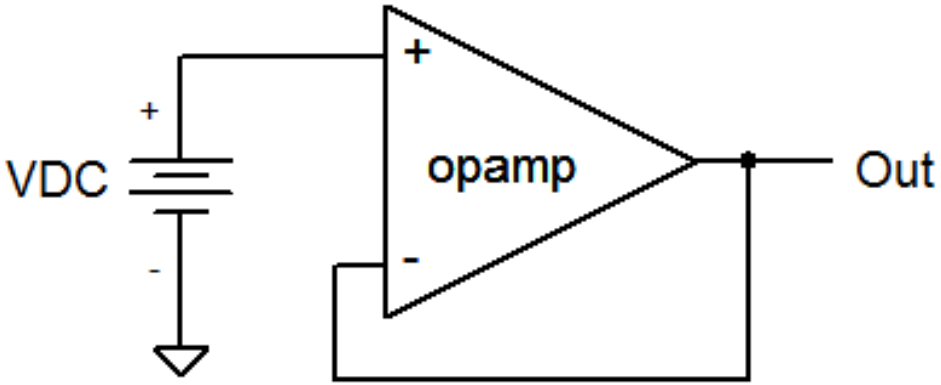
Input offset voltage

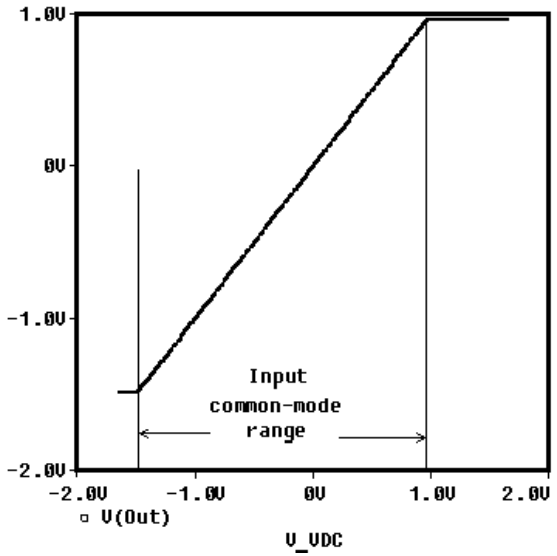




Op amps require a small voltage between their inverting and noninverting inputs to balance mismatches due to unavoidable process variations (*random offsets*) and to the specifics of the chosen circuit configuration (*systematic offsets*). The required voltage is known as the input offset voltage and is abbreviated Vos. Vos is normally modeled as a voltage source driving the noninverting input. Figure shows the typical methods for simulation of systematic input offset voltage by grounding the inverting input and DC sweeping the non-inverting. The right graph presents how the input offset can be determined – this is the value of input voltage at which the output voltage is a zero.

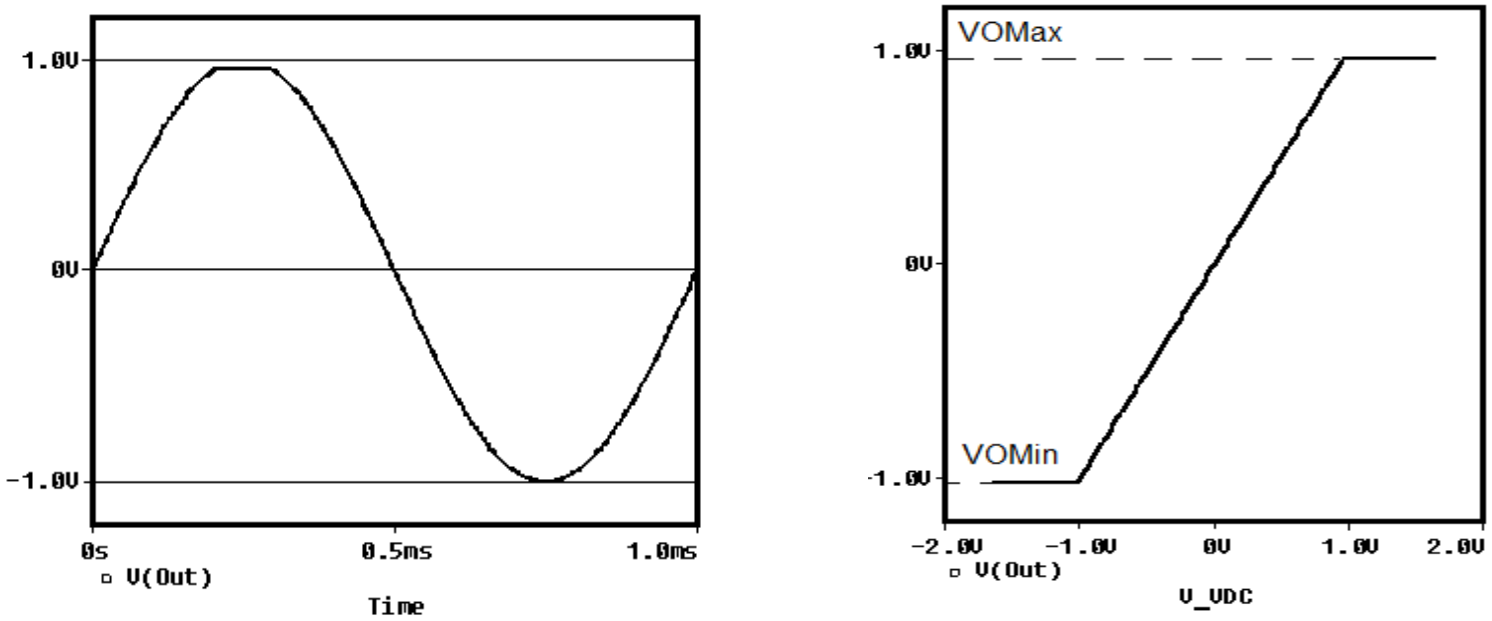
Input Common Mode Voltage Range





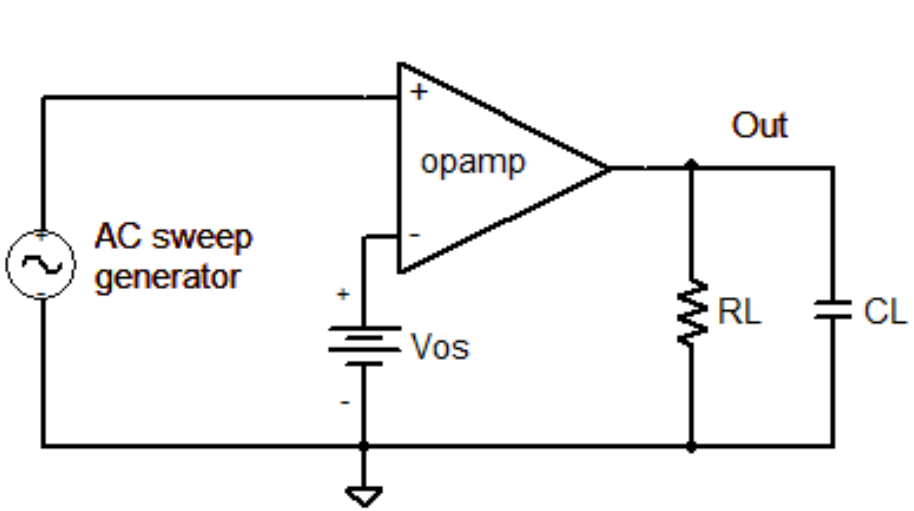
The input common voltage is defined as the average voltage at the inverting and noninverting input pins. If the common mode voltage gets too high or too low, the inputs will shut down and proper operation ceases. The common mode input voltage range, VICR, specifies the range over which normal operation is guaranteed. Figure shows the test circuit to obtain the unity-gain transfer characteristic of op amp. The graphic present the unity-gain transfer function and demonstrates the determination of the input common-mode voltage range.

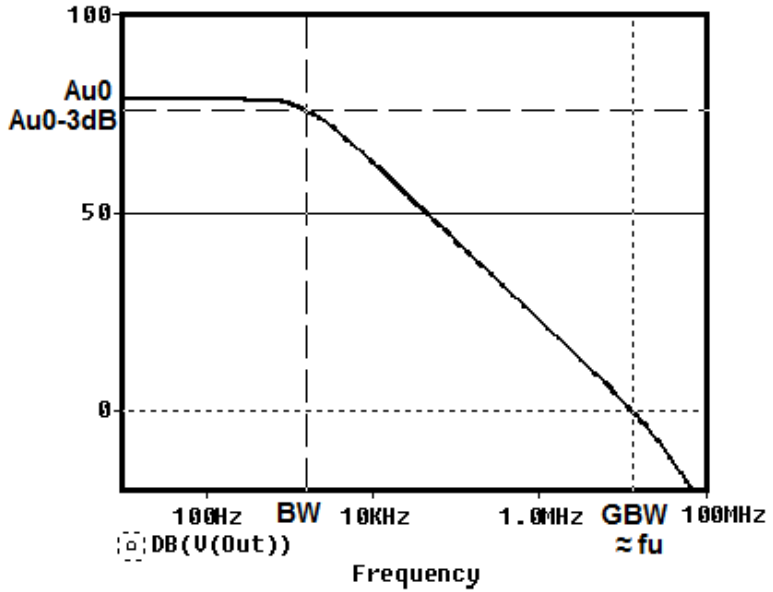
Maximum output voltage swing



The maximum output voltage is defined as *the maximum positive or negative peak output voltage* that can be obtained without wave form clipping, when quiescent DC output voltage is zero. VOMax and VOMin are limited by the output impedance of the amplifier, the saturation voltage of the output transistors, and the power supply voltages. VOMax and VOMin are not obligatory with opposite values. This is demonstrated on the left picture – the positive half-wave is clipped while the negative is undisturbed, i.e. |VOMin| > VOMax. The considered limits can be obtained from unity-gain transfer function as it is shown on the right plot. In order to get meaningful results, the anticipated loading can be connected to the output.

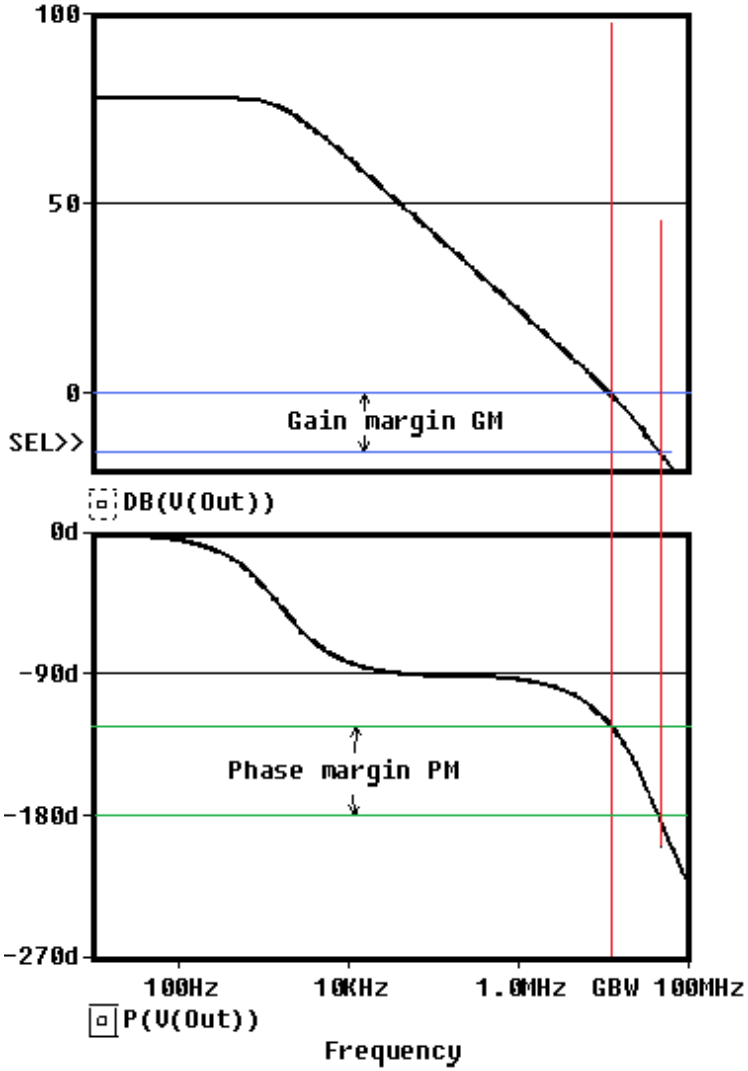
Open-loop gain, BW and GBW





One of the more important characterization of op amp performance is operation in the open-loop mode. The left picture propose a circuit for simulation testing of the open-loop gain. To this aim the frequency response of the op amp is investigated. The right plot shows a typical frequency response characteristic. At low-frequencies the open-loop gain **Au0** has a stable value about 80dB. The frequency, at which the gain starts decreasing is called the bandwidth **BW** or the **−3dB** frequency. The product of the low-frequency gain and the bandwidth is called the Gain-Bandwidth product **GBW**. Its value is very closed to unity gain frequency **fu** - the frequency, at which the gain is equal to 1 (0dB).

Phase margin and Gain margin

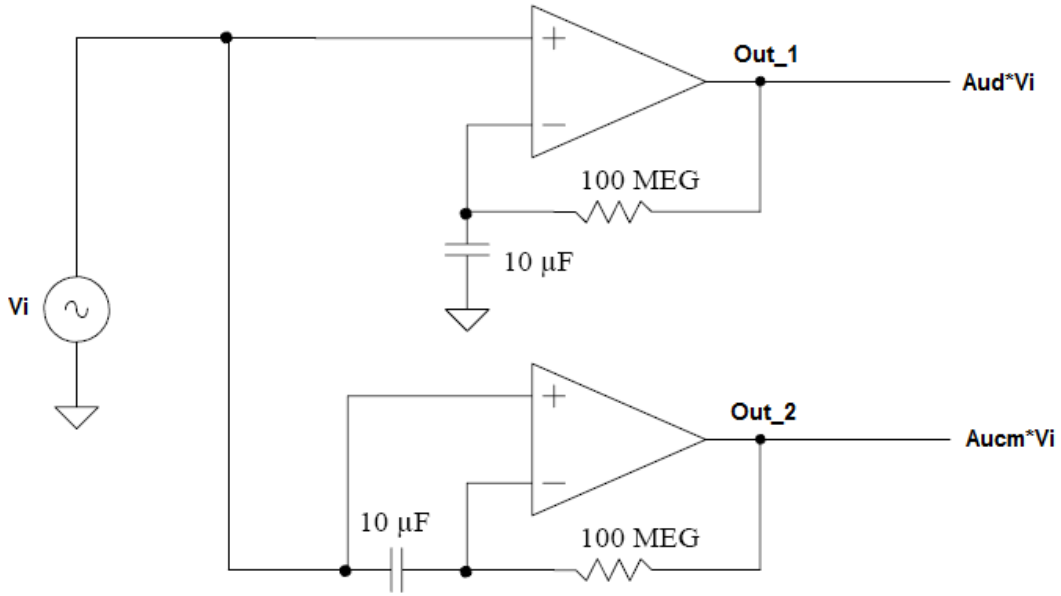


The upper plot shows the open-loop frequency response of the Op Amp. The lower plot presents its phase characteristic.

The left red line crosses the open-loop gain curve at 0dB and GBW frequency. The same line crosses the phase curve and determine the phase shift of the output signal (in this case about 120°). The difference between the value of the phase shift and the critical −180° is known as Phase margin **PM** (see the both green lines). For frequency stability of the Op Amp the phase margin should be higher than 45°. Otherwise the oscillations will appear.

Another parameter, which present the stability of the amplifier is the Gain margin **GM**. It is defined as the difference between unity gain and the gain at 180 phase shift (see the both blue lines).

Common mode rejection ratio

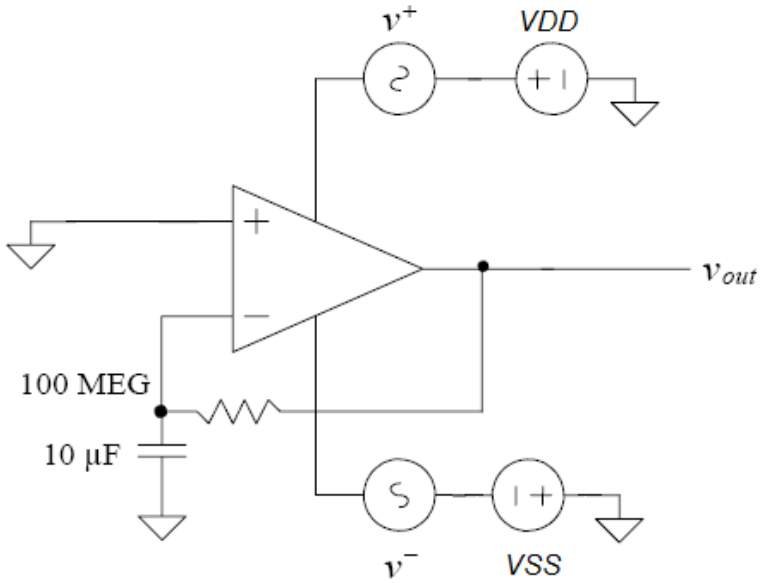


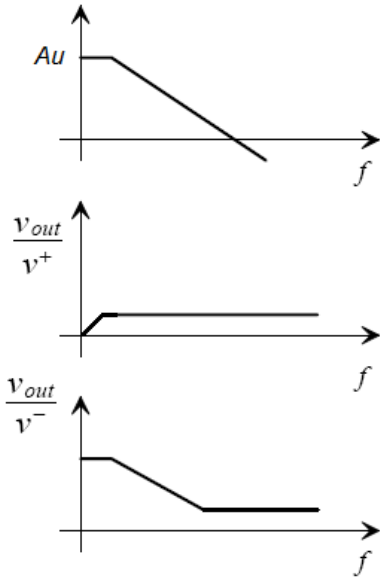
Common-mode rejection ratio, **CMRR**, is defined as the ratio of the differential voltage amplification **Aud** to the common-mode voltage amplification **Aucm**. Ideally this ratio would be infinite with common mode voltages being totally rejected.

The figure shows the test-circuit for CMRR simulation. The formula for CMRR calculation is

$$\mathrm{CMRR} = 20\log\left(\frac{A_{ud}}{A_{ucm}}\right) = 20\log\left(\frac{V(\mathrm{Out\_1})}{V(\mathrm{Out\_2})}\right).$$

Power supply rejection ratio



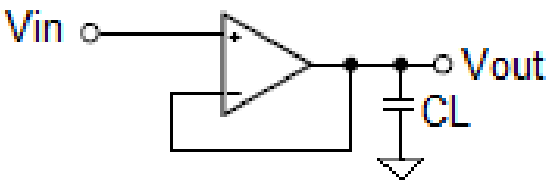


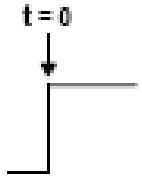
The power supply rejection ratio, **PSRR**, describes how well an amplifier rejects noise or changes on the VDD and VSS power supply. The figure shows the test-circuit for PSRR simulation. The formulas for PSRR calculation are

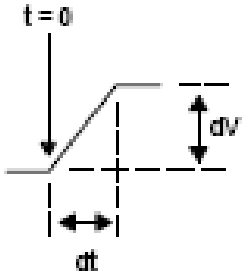
$$\mathrm{PSRR}^{+} = \frac{\mathrm{Au}}{\mathrm{v_{out}} / \mathrm{v}^{+}}; \quad \mathrm{PSRR}^{-} = \frac{\mathrm{Au}}{\mathrm{v_{out}} / \mathrm{v}^{-}}.$$

The right plots demonstrate the frequency characteristics of the three components of the above formulas.

Slew rate







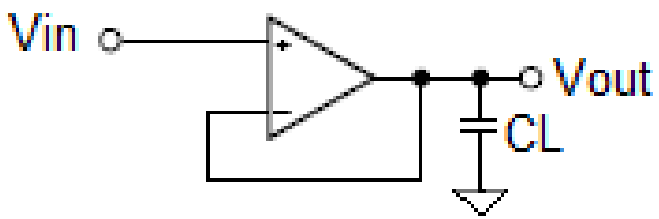
Vin Vout

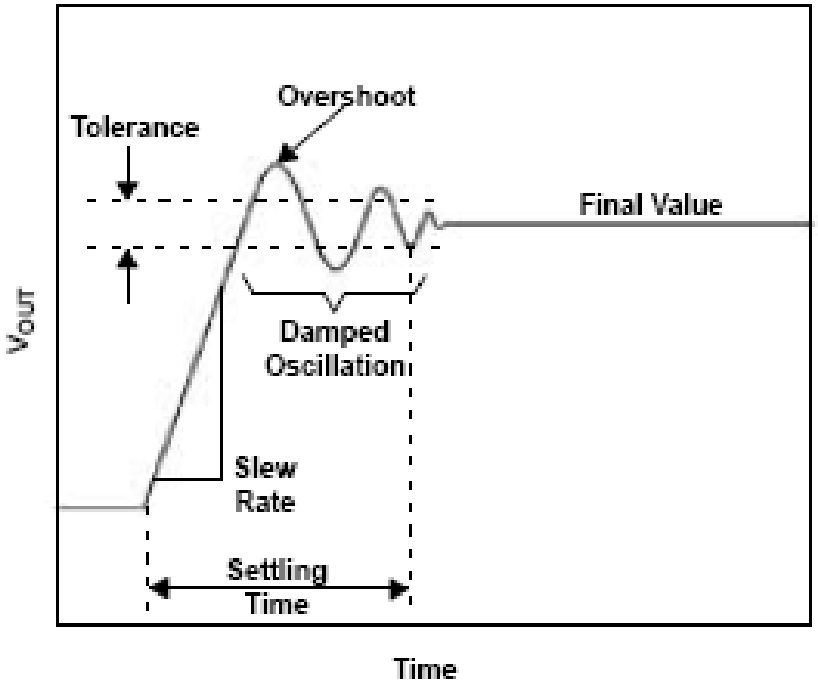
$$SR = \frac{dVout}{dt}$$

$$BOM = \frac{SR}{2\pi Vo\,min}$$

Slew rate, **SR**, is the rate of change in the output voltage caused by a step input. Its units are V/μs or V/ms. Figure shows slew rate graphically. The primary factor controlling slew rate in most op amps is the internal compensation capacitor Cc, which is added to make the op amp unity gain stable. In op amps without internal compensation capacitors, the slew rate is determined by the load capacitor CL. The slew rate is limiting factor for Maximum output-swing bandwidth, **BOM**. As the frequency gets higher and higher the output becomes slew rate limited and can not respond quickly enough to maintain the specified output voltage swing. BOM specifies the bandwidth over which the output is above a specified value Vomin.

Settling time



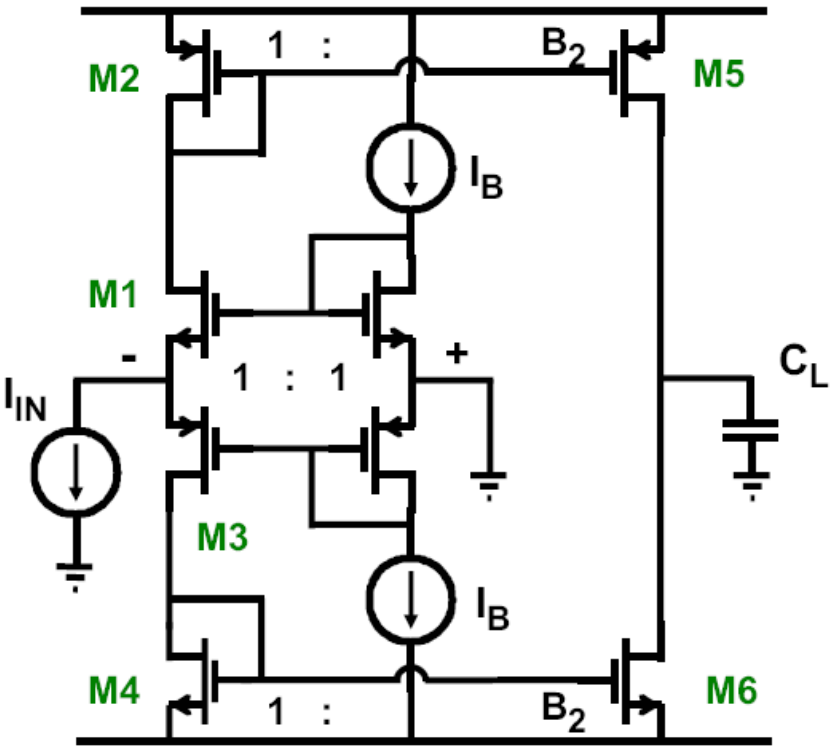


The settling time characterizes the finite time for a signal to propagate through the internal circuitry of an op amp. In fact it takes a period of time for the output to react to a step change in the input. In addition, the output normally overshoots the target value, experiences damped oscillation, and settles to a final value. Settling time, **ts**, is the time required for the output voltage to settle to within a specified percentage of the final value given a step input. Figure shows this graphically. Settling time is a design issue in data acquisition circuits when signals are changing rapidly.

Typical parameters of 0.25 μm OTA

Feature	Value	Unit
DC gain	80	dB
CMRR	40	dB
Offset	4-6	mV
Bandwidth	100	MHz
Slew-rate	3	V/μs
Settling time: 1 V, C_L = 4 pF	300	ns
PSRR @ DC	90	dB
PSRR @ 1 kHz	60	dB
PSRR @ 100 kHz	30	dB
Input referred noise (white)	100	nV/√Hz
Corner frequency	1	kHz
Supply voltage	3.3	V
Input common mode voltage	1.5	V
Output dynamic range	2.2	V_{pp}
Power consumption	1	mW
Silicon area	2000	μm^2

Operational current amplifier

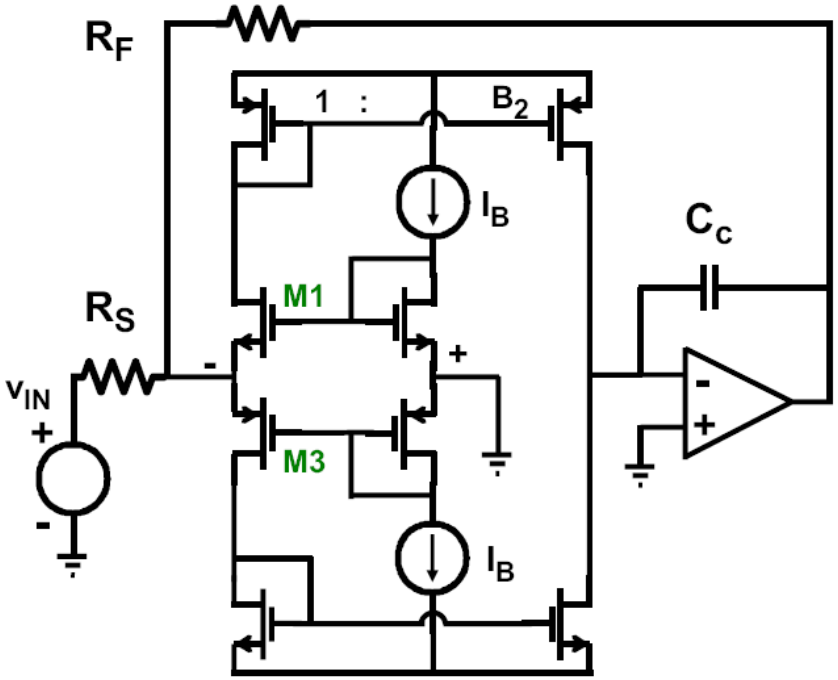


$$A_R = B_2 r_{out} = \frac{B_2}{g_{o5} + g_{06}}; \quad BW = \frac{1}{2\pi C_L r_{out}};$$

$$A_R BW = \frac{B_2}{2\pi C_L}; \quad SR = B_2 \frac{I_{in}}{C_L}$$

The Operational current amplifiers **OCA** uses of input common-gate stages M1 and M3, which are biased at current $\mathbf{I_B}$. The signals from the drains of M1 and M3 are current mirrored to the output, with current factor $\mathbf{B_2}$. For small-signals, the input current $\mathbf{i_{IN}}$ is divided over both input transistors, multiplied by $\mathbf{B_2}$, and generates an output voltage in the output resistance $\mathbf{r_{out}}$. The current gain is very modest ($\mathbf{B_2}$) but the transresistance ($\mathbf{A_R}$) can be very large. It is not possible to compare the product $\mathbf{A_R BW}$ to the **GBW** of a voltage amplifier. They have totally different dimensions. The main advantage of this amplifier is that the Slew Rate is unlimited. Indeed, for a large input current, the **SR** is determined by this input current itself, multiplied by $\mathbf{B_2}$.

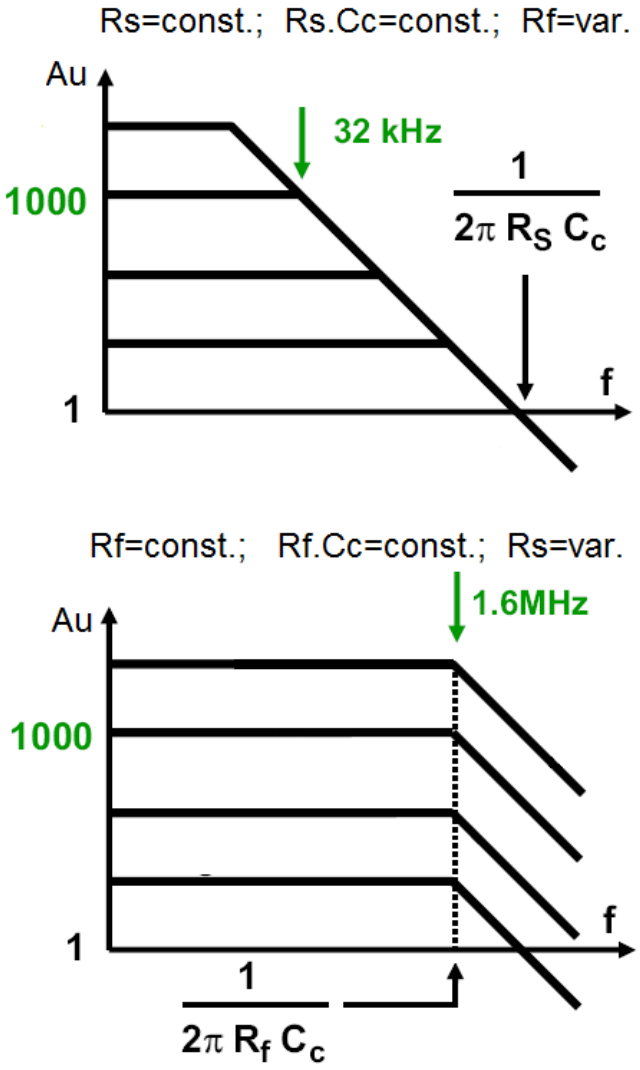
Operational current mode amplifier



The presented two-stage opamp has a OCA as a input stage and standard voltage-to-voltage stage as a second stage. Such operational amplifiers are known as Operational current-mode amplifiers CMA. In this circuit the low-voltage gain $\mathbf{A_{u0}}$ is defined from $\mathbf{R_F/R_S}$ ratio, as in voltage-to-voltage Op Amps. However, due to the current feedback, the expressions for the bandwidth are now different. The **BW** is determined by the feedback resistor $\mathbf{R_F}$, while the series resistor $\mathbf{R_S}$ controls the **GBW**.

$$A_u = -\frac{R_F}{R_S}\frac{1}{1+j\omega R_F C_C};\quad A_{u0} = -\frac{R_F}{R_S};\quad BW = \frac{1}{2\pi R_F C_C};\quad GBW = \left|A_{u0}\right|\cdot BW = \frac{1}{2\pi R_S C_C}$$

Current feedback - example

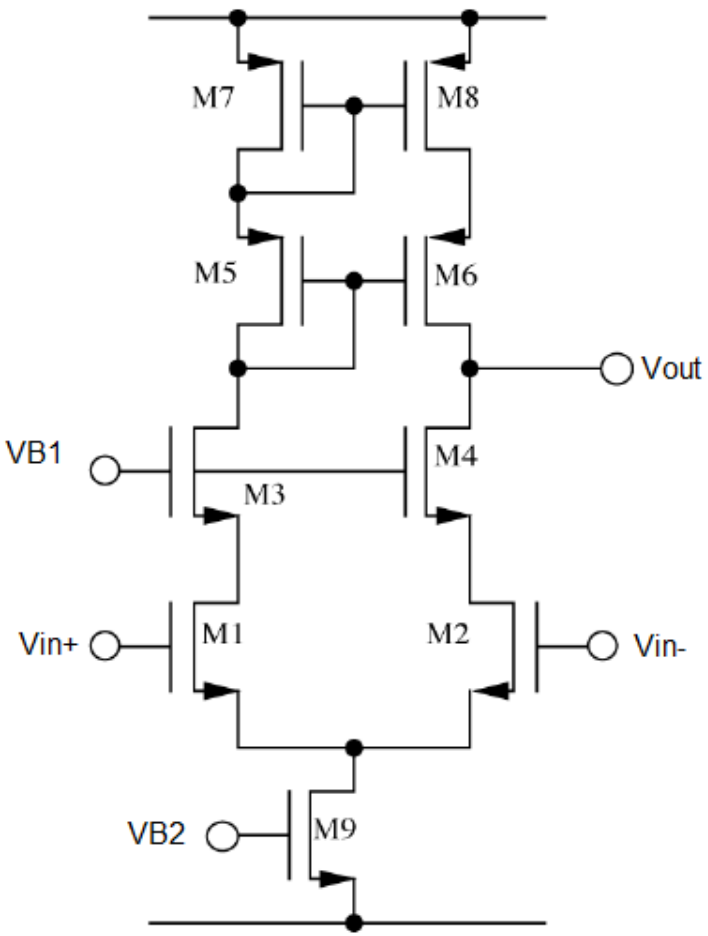


The graphics demonstrate the frequency response of the CMA. The upper plot is for the case in which, the resistor Rs=const. Then, the product RsCc is a constant too and the GBW has a fixed value, independent on the Rf. Rf is used for control of the gain. The characteristics are exactly the same set of curves as for a voltage opamp, but the gain and the GBW can be controlled separately.

The lower plot demonstrates the case in which Rf is kept a constant and as an result fixes the BW of the amplifier. The gain can be controlled by changing of the Rs.

It is clear that with this current mode opamp, we can reach combinations of large gain and high speed, which are not available with a conventional voltage op amp. This is a basic advantage of this circuit.

Telescopic cascode single stage OTA



To improve the gain of the voltage amplifiers the cascode stage can be added. For example, four cascode MOSTs M3–M6 are added in series with the input devices and current mirror, as is shown in this slide. This is called the telescopic cascode CMOS OTA. The impedance at the output node increases considerably, and consequently the gain, but not the GBW. The power consumption does not increase. Without cascodes, the gain is moderate. With cascodes however, the gain is increased, but only at low frequencies. Cascode transistors are now mainly used for more gain at low frequencies, for example for lower distortion at low frequencies.

For deep submicron or nanometer CMOS this solution has always become a necessity, as the gain per transistor has become less than 10.

Micro-power OTAs

The portable systems require very low power consumption. The way to achieve that is to minimize the current (consequently, the power) in the basic blocks used. When the bias current in a MOS transistor becomes pretty low, the region of operation is no more the saturation but transistor enters in the sub-threshold region where the current-voltage relationship is exponential and the transconductance of the transistors and respectively the gain of a simple inverter with active load becomes

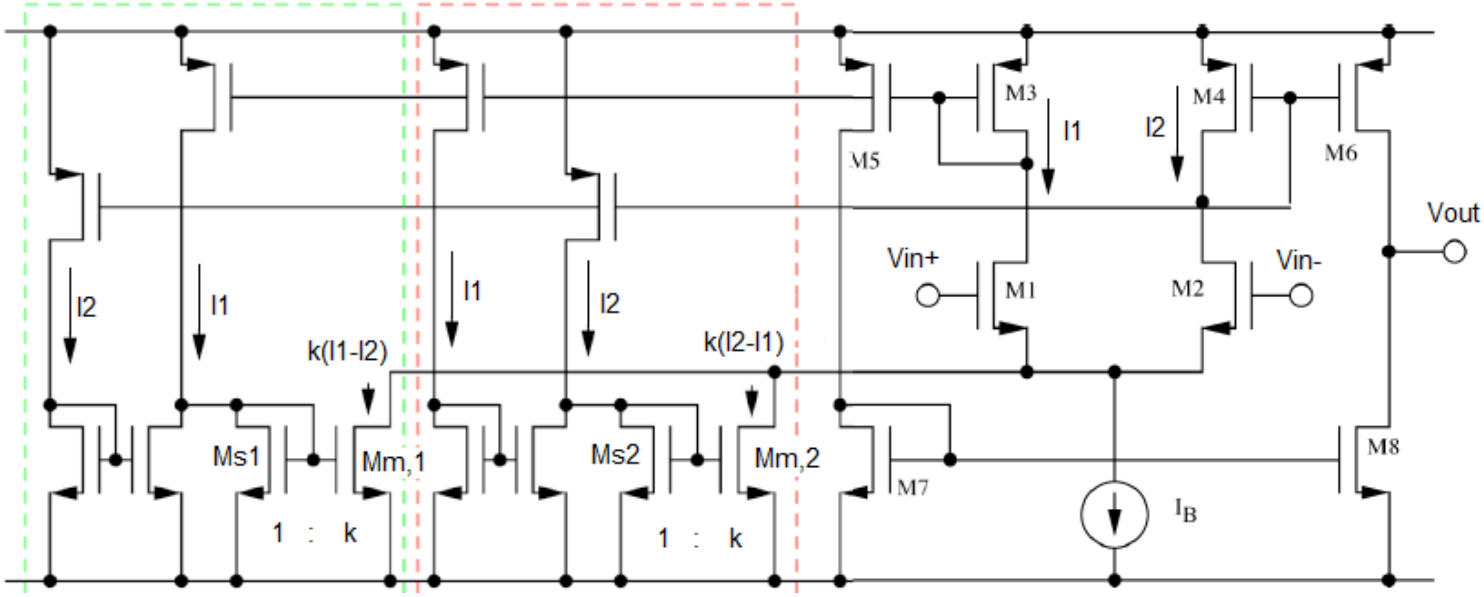
$$g_m = \frac{I_d}{n\varphi_T} \qquad A_u = \frac{-1}{n\varphi_T\left(\lambda_n + \lambda_p\right)}$$

At room temperature, the gain can be around 60 dB, but, because of the very small currents, the bandwidth is limited and, more important, small currents lead to small slew-rates - this is, normally, the most severe design limitation.

Therefore, when designing a micro-power OTA it is necessary to use specific techniques to entrance the slew-rate. The designer can use two methods:

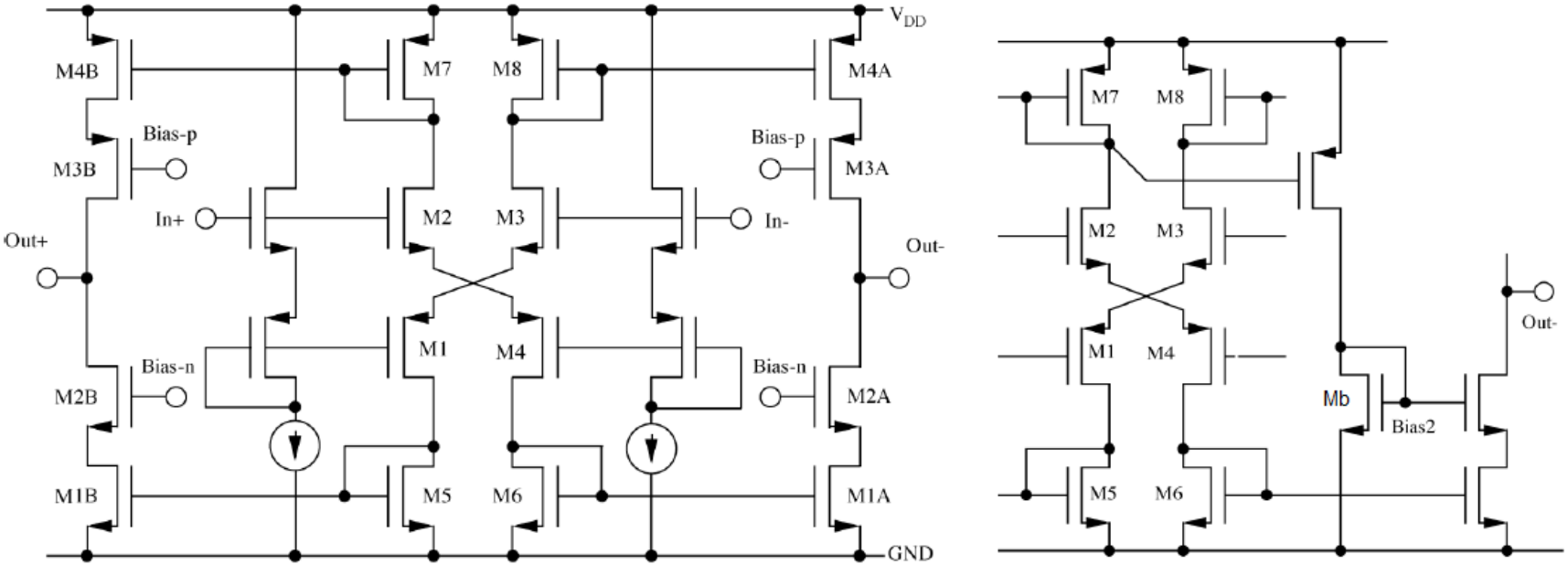
- dynamic biasing of the current tail and
- dynamic voltage biasing in push-pull stages.

Dynamic biasing of the current tail



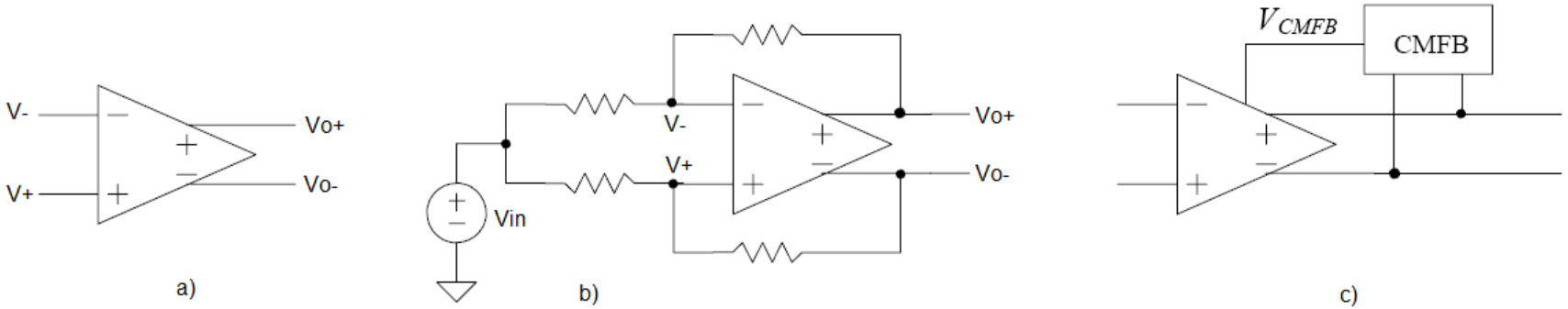
The basic concept behind dynamic biasing is to provide more current than the quiescent level when slewing needs it. To achieve the result it is necessary to use a slew-rate detector and to have a current bias boost. In the slew-rate region the current in one branch of the input differential stage equals the tail current while the current in the other branch goes to zero. Thus, we detect the slew-rate condition by measuring the full current unbalancing in the input differential stage. Hence, the circuit inside the green dashed lines takes the difference between I1 and I2 currents and that, if positive, flows into the sensing transistor Ms,1. The similar circuit (in red dashed line) permits us to sense I2-I1 (if positive). The combination of the two results, formed by the mirroring elements Mm,1 and Mm,2, provide k|I1-I2|, where k comes from the mirror factors used.

Dynamic voltage biasing in push-pull stages



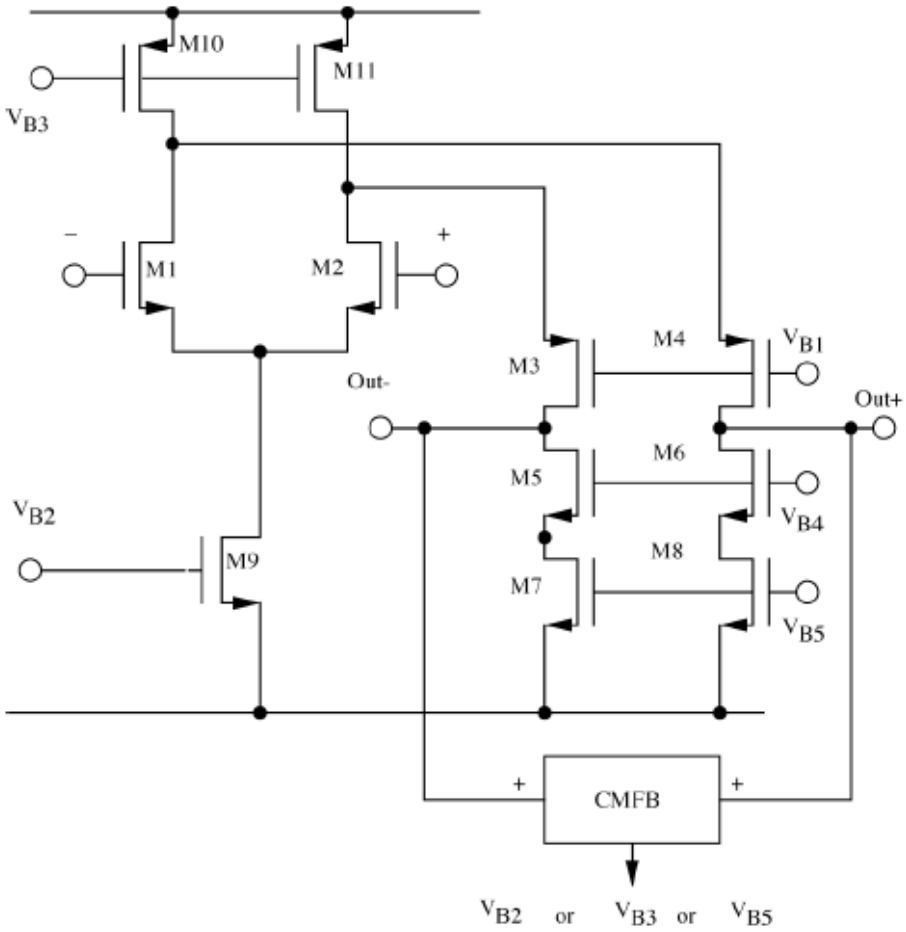
A push-pull scheme allows the use of very low currents and works with relatively low supply voltages. The AB class operation also provides large current when the op-amp is required to sustain the slewing phase. The main design problem concerns the bias of the cascode transistors. For maximum output swing the bias voltages Bias-n and Bias-p must approach as close as possible to the rail voltages. However, during the slewing the current sources of the output cascodes can be pushed in the linear region and loosing the advantage of the AB operation. The problem is solved with the dynamic biasing (the right figure). During slewing the I_{M6} increases, which leads I_{M7} growths. Then the augmented bias current in Mb pulls up Bias2. This happens until the circuit remains in the slewing phase. In the normal conditions I_{M7} returns to its quiescent level and Bias2 goes back to the nominal value.

Fully differential op amp



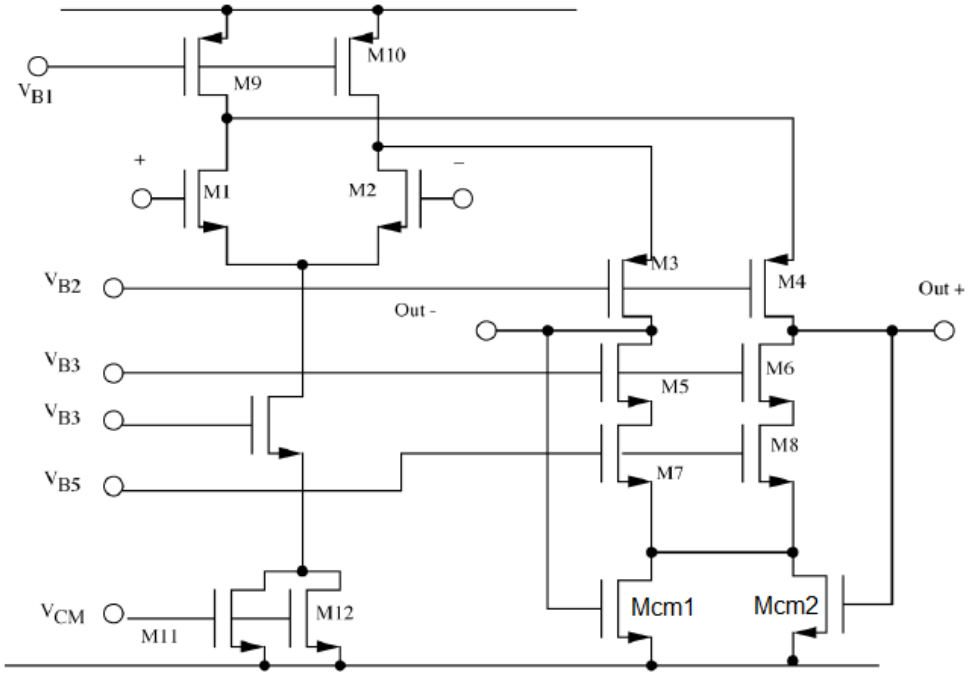
The figure a) presents the fully differential op amp. It have a differential input and produce a differential output. The fully differential op amps are widely used in modern integrated circuits because provide a larger output voltage swing and are less susceptible to common mode noise. Also, if the circuit is balanced (perfectly matched towards all axis of symmetry) even-order nonlinearities are not present. The specific of fully differential op amps is that require two matched feedback networks and a common-mode feedback circuit to control the common-mode output voltage. Figure b) shows a simple differential output op-amp gain configuration. This circuit utilizes the two input terminals to establish the feedback in both paths and consequently, it doesn't have any bind to analog ground. The dc gain ensures that the differential input is small or, at the limit, zero but there is no condition that fixes the quiescent voltage of input and output terminals. This make the common-mode output voltage Vcm floating. To fix the Vcm the configuration c) is used. The common-mode feedback circuit (CMFB) senses the average value of the op-amp outputs. The CMFB output is fed back into the op-amp to adjust Vcm to the correct value - usually (VDD+VSS)/2.

Fully differential OTA with CMFB



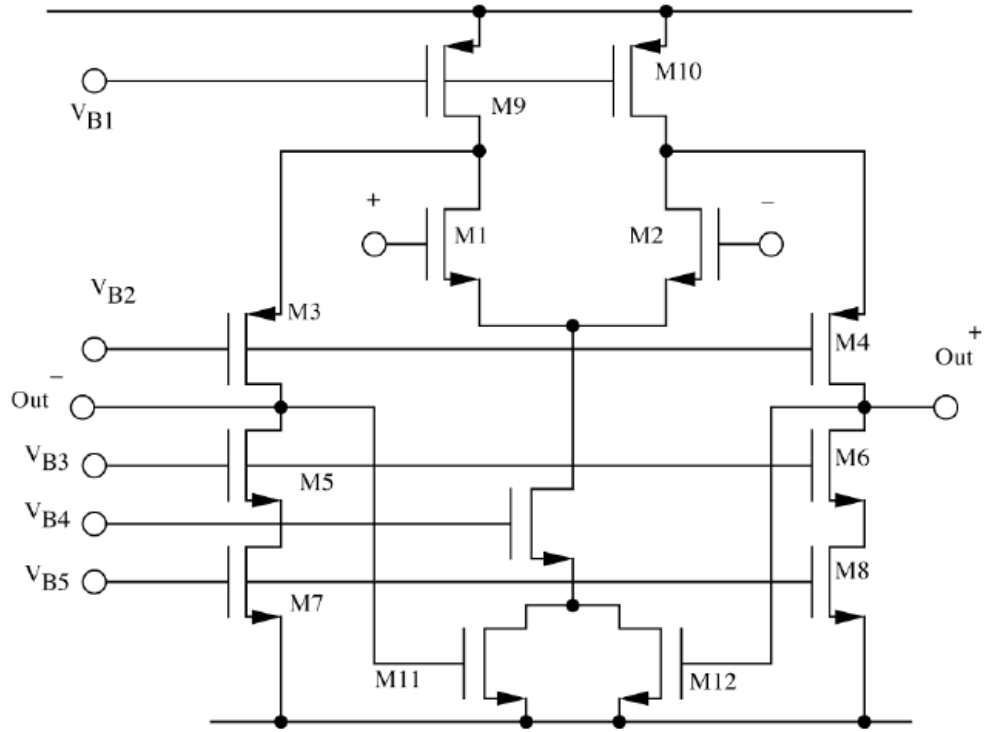
The figure shows the fully differential version of the folded cascode OTA. In this circuit we need to properly bias transistor pairs M3-M4, M5-M6 and M7-M8. The schematic highlight the points where the designer can introduce the common-mode feedback. We can achieve the necessary balance of currents by adjusting in feedback the gate voltages VB2, VB3 or VB5.

Fully differential folded cascode with CMFB -1



In the presented circuit the common-mode feedback is implemented with transistors Mcm1 and Mcm2. They operate in linear region as resistors. If Vout is positive towards the fixed Vcm, the resistance of the Mcm1 and Mcm2 decrease and the output voltage go down. And vise versa – if Vout is smaller than the fixed Vcm, the resistance of the Mcm1 and Mcm2 increase and the output voltage go up.

Fully differential folded cascode with CMFB -2



The figure presents another variant of CMFB. In this case transistors M11 and M12 control the current to the input differential pair. If Vout increases, the quiescent current increase too, the voltages at the output of the M1 and M2 decrease and compensate the growth of the output voltage.

Instructions for self-study

The past presentation gives only a first sight on the hand-calculation models for CMOS active devices. After reading and understanding the presented information you have to study the material from at least one of the following textbooks:

- R. Baker, H. Li, D.Boyce. CMOS Circuit Design, Layout and Simulation, IEEE Press, New York, 2005, ISBN 0-7803-3416-7. Chapter 25, pp.617-682.

- Ph. E. Allen, D. R. Holberg. CMOS Analog Circuit Design, Oxford University Press, Inc., 2002. ISBN 0-19-511644-5, Chapter 6, pp. 243-351, Chapter 7, pp. 352-438.

- F. Maloberti. Analog design for CMOS VLSI Systems. Kluwer Academic Publishers, 2003, eBook ISBN: 0-306-47952-4, Print ISBN: 0-7923-7550-5, Chapter 5, pp.217-324.

The next step in the learning process is to study the examples and complete the experiments, which are presented in Non-guided exercise 5